CUSTOMER	
MODEL	WD-F9624W3-7FLWa VER. 2
CUSTOMER APPROVED	

APPROVED BY	CHECKED BY	ORGANIZED BY
LCM 產品部 2010/4/12 曾憲章	LCM 產品部 2010/04/10 夏勝華	LCM 產品部 2010/4/9 羅倩

☐ APPROVAL FOR SPECIFICATIONS ONLY

☒ APPROVAL FOR SPECIFICATIONS AND SAMPLE 10030384

History of Version

Version	Contents	Date	Note
a1	New version	18.Mar.2010	spec.
a2	Change by customer 1. Add Sample NO:10030384(參照WD-F9624VU-7FLWa 只改檢驗規格爲LM-I-0018) 2. Modify 3.3 Packing Method	08.Apr.2010	spec.& sample

Contents Page

(1) Electronic Units

1.1 Absolute Maximum Ratings

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Operating Temperature	TOP	-20	-	+70	℃
Storage Temperature	TST	-30	-	+80	℃
Supply Voltage for System	VCI-VSS	-0.3	-	+5.0	V
Static Electricity	Be sure that you are grounded when handing LCM.				

1.2 Electrical Characteristics

(Ta=25℃)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage for System	VCI	-	3.0	3.3	3.6	V
Positive Power for Scan Driver	VGH	-	14	15	16	V
Negative Power for Scan Driver	VGL	-	-11	-10	-9	V
Input Signal High Voltage	VIH	-	0.7VCI	-	VCI	V
Input Signal Low Voltage	VIL	-	VSS	-	0.3VCI	V
Output Signal High Voltage	VOH	-	-	-	-	V
Output Signal Low Voltage	VOL	-	-	-	-	V
Supply Current for System	*ICI	Fr=65Hz	-	6.2	8	mA
Used IC	NT53005					

*ICI Measurement condition is for all pixels on
*IDD Measurement condition is for all pixels on

1.3 Interface Pin Function

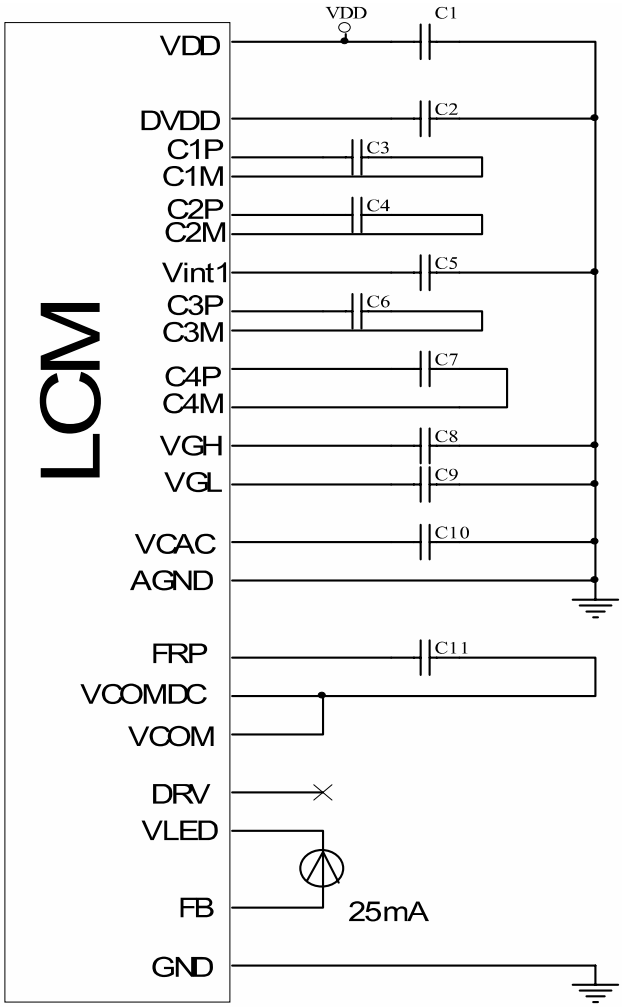
CN1:

NO	SYMBOL	I / O	FUNCTION
1	VCOM	I	Common electrode driving voltage
2	CS	I	Serial communication chip select
3	SDA	I/O	Serial communication data input/output
4	SCL	I	Serial communication clock input
5	HSYNC	I	Horizontal sync input
6	VSYNC	I	Vertical sync input
7	DCLK	I	Clock input
8	D7	I	Data input: MSB
9	D6	I	Data input
10	D5	I	Data input
11	D4	I	Data input
12	D3	I	Data input:
13	D2	I	Data input
14	D1	I	Data input:
15	D0	I	Data input: LSB
16	GND	P	Digital GND
17	VDD	P	System power(VDD=VCI=3.3V)
18	DVDD	C	Power setting capacitor connect pin
19	C1P	C	Power setting capacitor connect pin
20	C1M	C	Power setting capacitor connect pin
21	C2P	C	Power setting capacitor connect pin
22	C2M	C	Power setting capacitor connect pin
23	Vint1	C	Intermediate voltage for charge Pump
24	C3P	C	Power setting capacitor connect pin
25	C3M	C	Power setting capacitor connect pin
26	NC	-	Not connection
27	NC	-	Not connection
28	C4P	C	Power setting capacitor connect pin
29	C4M	C	Power setting capacitor connect pin
30	VGH	C	Positive power supply for gate output::+15V
31	VGL	C	Negative low power supply for gate output:-10V
32	AGND	P	Ground for analog circuit
33	FPR	O	Frame polarity output for VCOM
34	COMDC	O	VCOM DC voltage output pin
35	VCAC	C	Define the amplitude of the VCOM swing
36	DRV	O	Gate signal for the power transistor of the boost converter

37	VLED	P	For Led Anode voltage
38	FB	P	LED power cathode
39	VCOM	I	Common electrode driving voltage

1.4 Power Supply for LCD Module

1.4.1 With external LED driver circuit



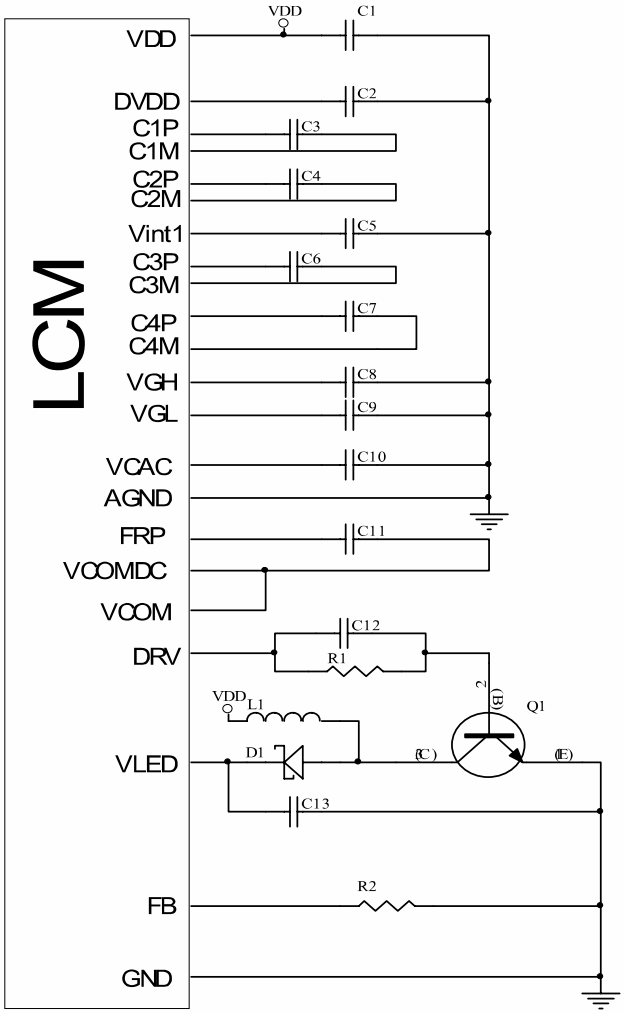
Note1: VDD=VCI=3.3V

The LED must be current driving. ILED=25mA

Pin name	Capacitor no.	Withstanding(V)	CAP(uF)
C1P-C1M	C3	10	≧2.2
C2P-C2M	C4	10	≧1
C3P-C3M	C6	16	≧1
C4P-C4M	C7	16	≧1
VDD	C1	6.3	≧1
DVDD	C2	6.3	≧1
VINT1	C5	10	≧2.2
VGH	C8	25	≧2.2
VGL	C9	16	≧2.2
VCAC	C10	10	≧2.2
FRP-VCOMDC	C11	10	≧2.2

Note2: Use external LED driver must set R5[1](SHDB1)=”0”

1.4.2 With internal LED driver circuit



Note1: VDD=VCI=3.3V,

The LED must be current driving. ILED=25mA

Pin name	Capacitor no.	Withstanding(V)	CAP(uF)
C1P-C1M	C3	10	≧2.2
C2P-C2M	C4	10	≧1
C3P-C3M	C6	16	≧1
C4P-C4M	C7	16	≧1
VDD	C1	6.3	≧1
DVDD	C2	6.3	≧1
VINT1	C5	10	≧2.2
VGH	C8	25	≧2.2
VGL	C9	16	≧2.2
VCAC	C10	10	≧2.2
FRP-VCOMDC	C11	10	≧2.2

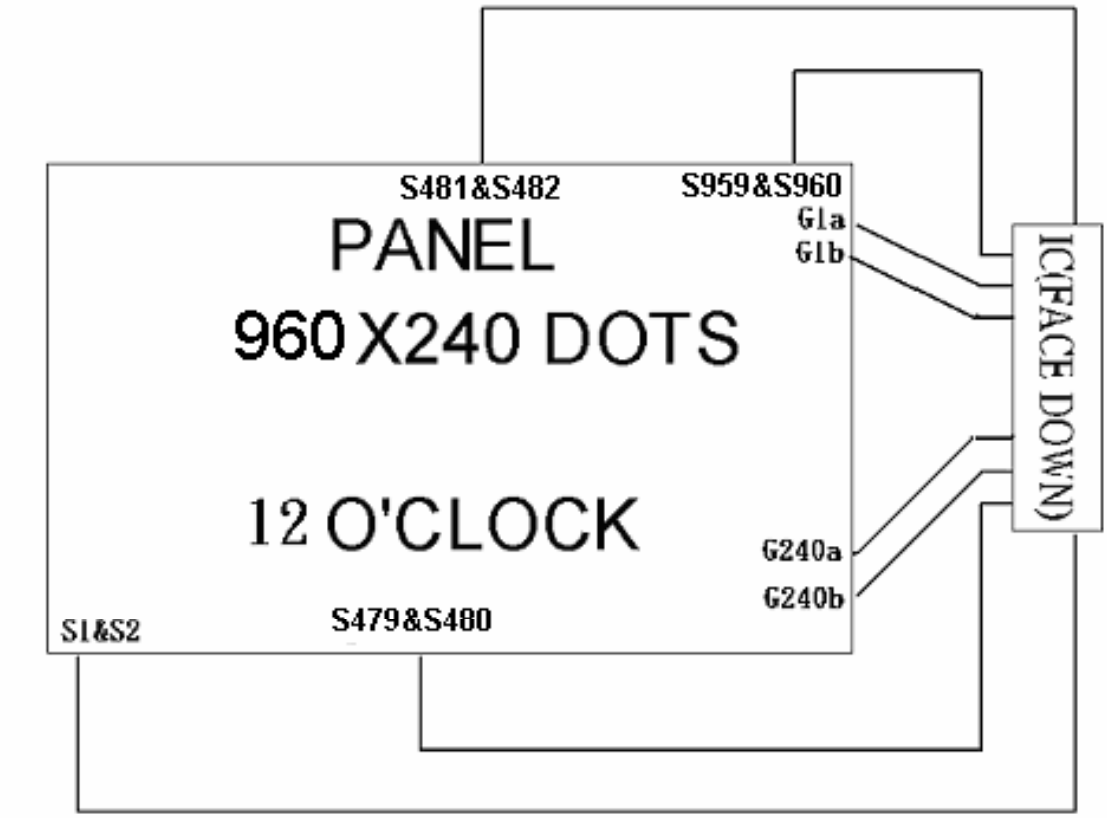
Note2: C12 =2.2nF/6.3V,C13 =10uF/16V,R1=10K ohm,R2=24ohm,L1=47uH

D1:RB521S-30, Q1:FMMT618

Note3: Use internal LED driver must set R5[1](SHDB1)=”1”

1.5 Block Diagram with Display RAM Address

1.5-1. Block Diagram



1.5-2. Initialization Table:

NO	Document Number	Attachment file
1	DF9624VI-IN1-103	

Double-Click the "Attachment Icon" above for opening attachment file.

1.6 Timing Characteristic

Timing Diagram

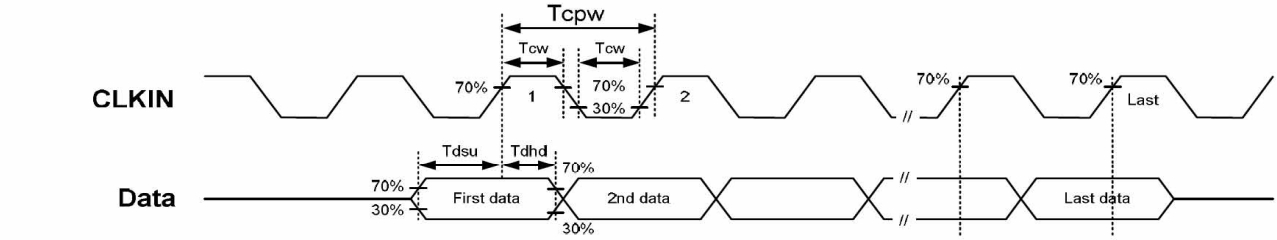


Figure 21. CLKIN vs. Data timing diagram

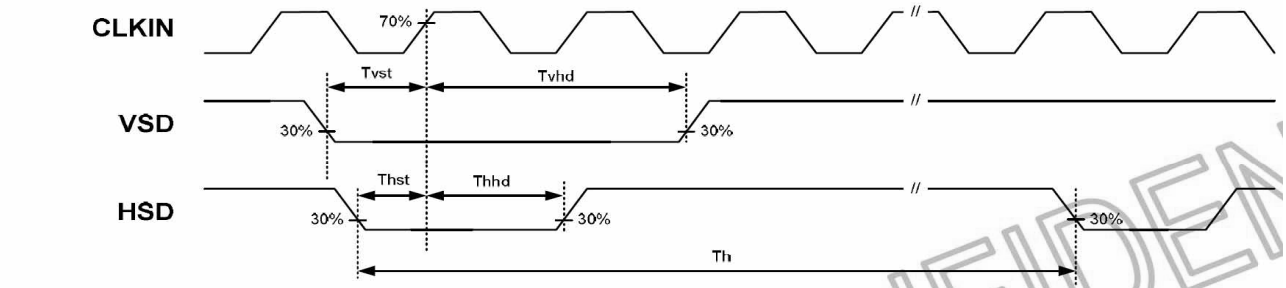


Figure 22. CLKIN vs. HSD & VSD timing diagram

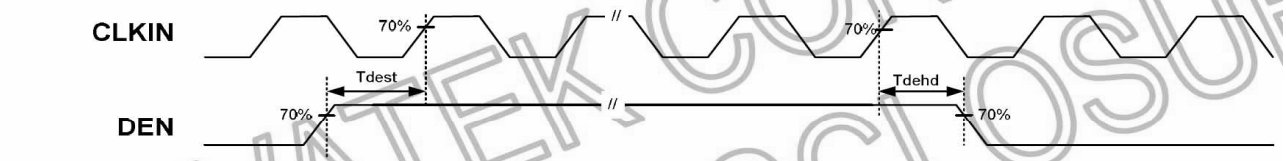


Figure 23. CLKIN vs. DEN timing diagram

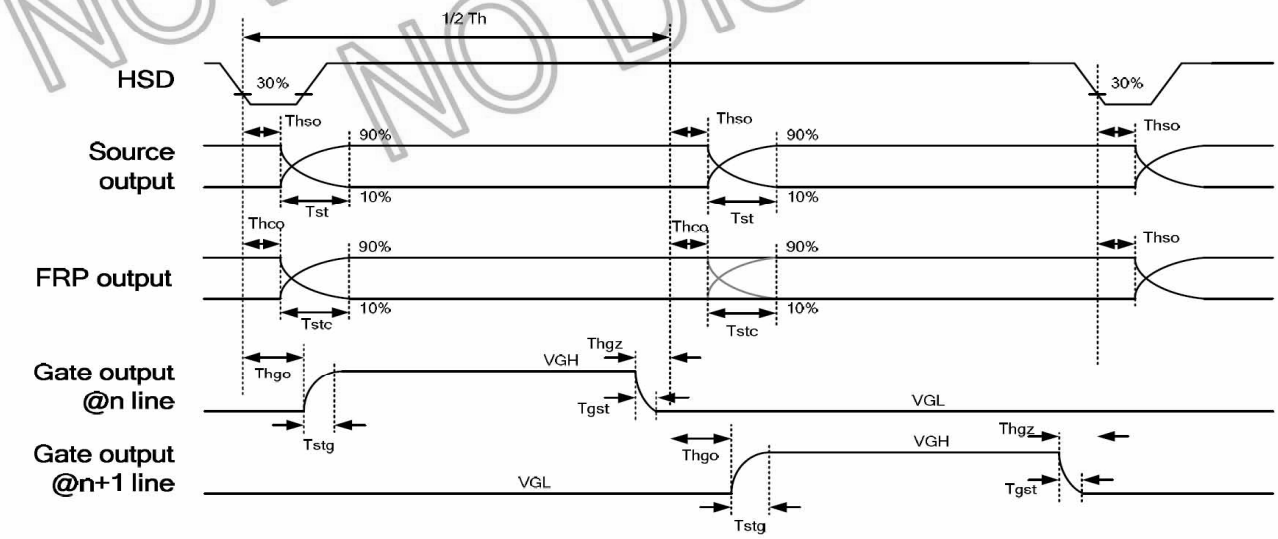


Figure 24. HSD vs. output timing diagram

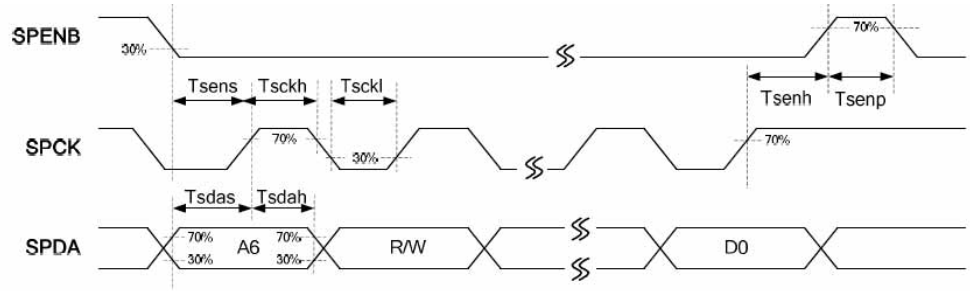


Figure 25. 3-Wire Serial interface timing diagram

14. Input Data Format

14.1. Vertical Timing Chart

14.1.1. HV Mode

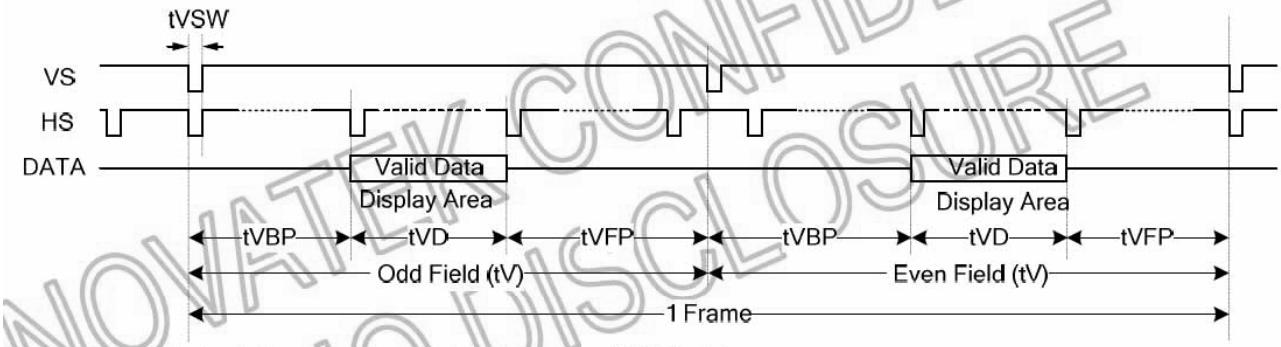


Figure 26. 8-bit Serial interface vertical timing chart (HV Mode)

14.1.2. DE Mode

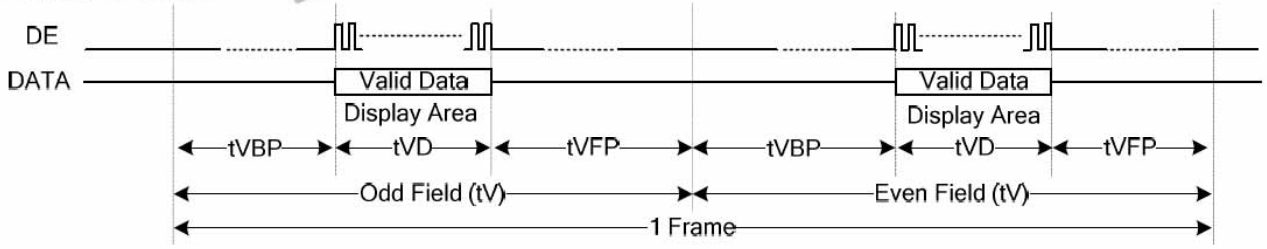


Figure 27. 8-bit Serial interface vertical timing chart (DE Mode)

14.2. Horizontal Timing Chart

14.2.1. HV Mode

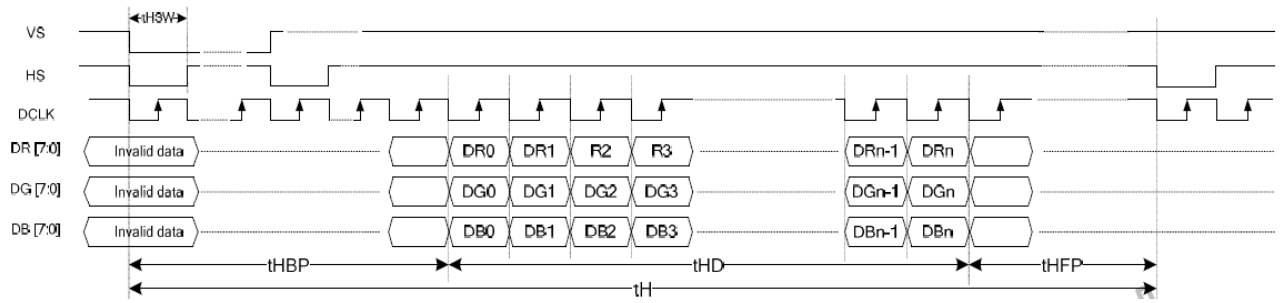


Figure 28. 8-bit Serial interface Horizontal Timing Chart (HV Mode)

14.2.2. DE Mode

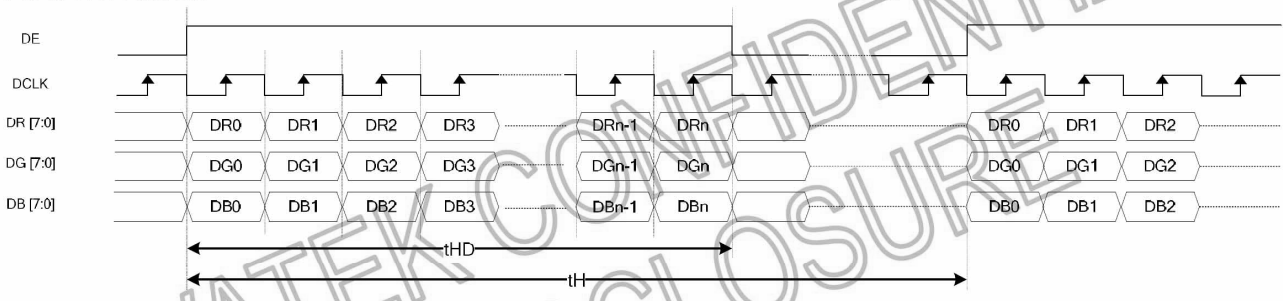


Figure 29. 8-bit Serial interface Horizontal Timing Chart (DE Mode)

14.3. Input Data Format Table
14.4. 8-bit RGB/YUV/CCIR Input Data Format

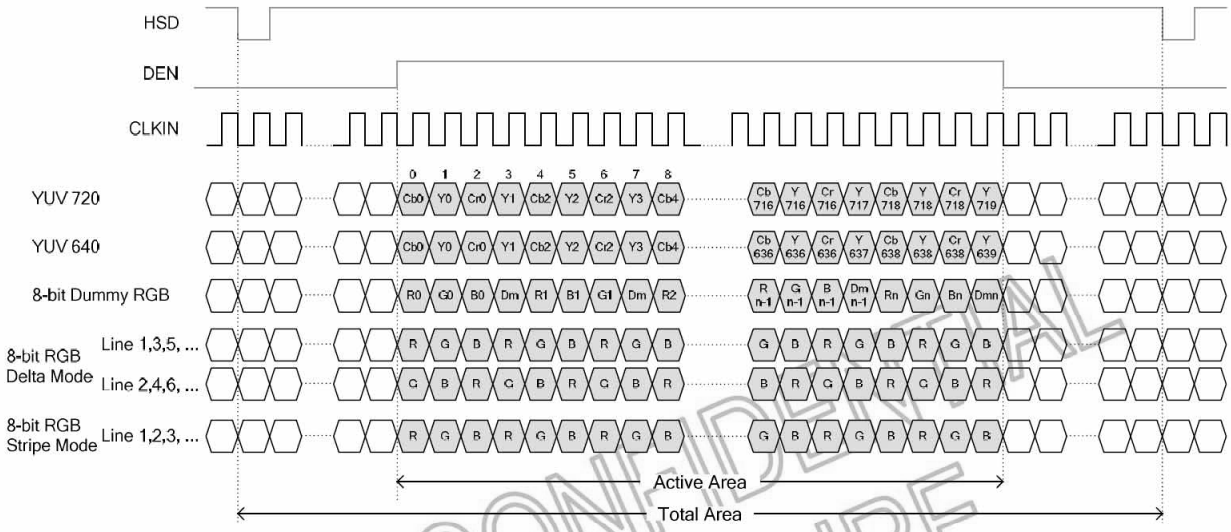


Figure 30. 8-bit Serial interface Input Data Format

14.5. 8-bit RGB Input Timing

Table 55. 8-bit RGB Input Timing Table

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	14	27	30	MHz
HSD period		tH	990	1716	1728	CLKIN
HSD display period		tHD		960		CLKIN
HSD back porch		tHBP	16	70	255	CLKIN
HSD front porch		tHFP	14	686	718	CLKIN
HSD pulse width		tHSW	1	1	128	CLKIN
VSD period time		tV	244.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	6	H
1 Frame			489	525	901	H

14.6. 8-bit DUMMY RGB input timing

Table 56. 8-bit Dummy RGB (320 mode/NTSC/24.535Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20	24.535	30	MHz
HSD period		tH	1321	1560	1907	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	16	241	255	CLKIN
HSD front porch		tHFP	25	39	372	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	244.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	6	H
1 Frame			489	525	901	H

Table 57. 8-bit Dummy RGB (320 mode/PAL/24.375Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20	24.375	30	MHz
HSD period		tH	1321	1560	1920	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	16	241	255	CLKIN
HSD front porch		tHFP	25	39	385	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	294.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	6	H
1 Frame			589	625	901	H

Table 58. 8-bit Dummy RGB (360 mode/NTSC/27Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	22	27	30	MHz
HSD period		tH	1481	1716	1907	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	16	241	255	CLKIN
HSD front porch		tHFP	25	35	212	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	244.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	6	H
1 Frame			489	525	901	H

Table 59. 8-bit Dummy RGB (360 mode/PAL/27Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	22	27	30	MHz
HSD period		tH	1481	1728	1920	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	16	241	255	CLKIN
HSD front porch		tHFP	25	47	225	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	294.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD Front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	6	H
1 Frame			589	625	901	H

14.7. YUV720 and YUV640 input timing

Table 60. YUV 720 mode/NTSC input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	27	30	MHz
HSD period		tH	-	1716	-	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	16	240	255	CLKIN
HSD front porch		tHFP	-	36	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	-	H
	Even field		3.5	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	1	1	6	H
1 Frame			-	525	-	H

Table 61. YUV 720 mode/PAL input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	27	30	MHz
HSD period		tH	-	1728	-	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	16	240	255	CLKIN
HSD front porch		tHFP	-	48	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	312.5	-	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	24	-	H
	Even field		3.5	24.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	1	1	6	H
1 Frame			-	625	-	H

Table 62. YUV 640 mode/NTSC input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	24.535	30	MHz
HSD period		tH	-	1560	-	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	16	240	255	CLKIN
HSD front porch		tHFP	-	40	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	-	H
	Even field		3.5	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	1	1	6	H
1 Frame			-	525	-	H

Table 63. YUV 640 mode/PAL input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	24.375	30	MHz
HSD period		tH	-	1560	-	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	16	240	255	CLKIN
HSD front porch		tHFP	-	40	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	312.5	-	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	24	-	H
	Even field		3.5	24.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	1	1	6	H
1 Frame			-	625	-	H

14.8. 24-bit RGB Input Data Format

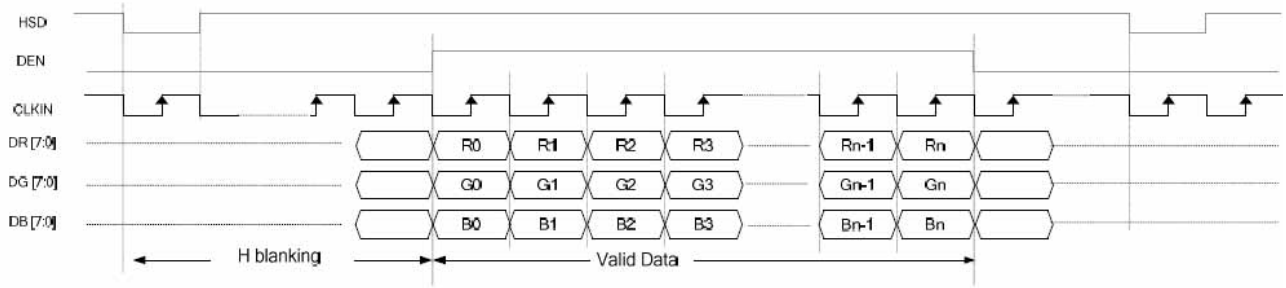


Figure 31. 24-bit RGB interface Input Data Format

14.9. 24-bir RGB Input Timing

Table 64. 24-bit RGB Input Timing Table

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	6.74	7.5	MHz
HSD period		tH	-	428	-	CLKIN
HSD display period		tHD		320		CLKIN
HSD back porch		tHBP	16	61	255	CLKIN
HSD front porch		tHFP	-	47	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	-	H
	Even field		3.5	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	1	1	6	H
1 Frame			-	525	-	H

14.10. CCIR_656 Mode Data format

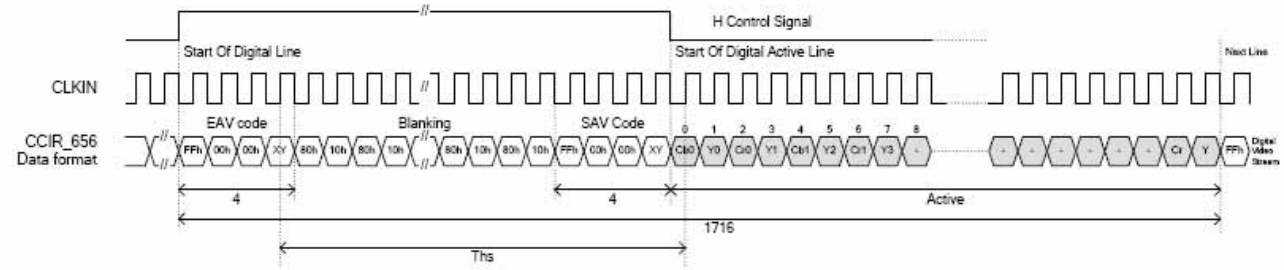


Figure 32. CCIR_656 Input Data Format

- FF 00 00 XY signals are involved with HSD,VSD and Field
- XY encode following bits:
  F=field select
  V=indicate vertical blanking
  H=1 if EAV else 0 for SAV
  P3-P0=protection bits :
  P3=V⊕H P2=F⊕H P1=F⊕V P0=F⊕V⊕H ⊕: Represents the exclusive-OR function

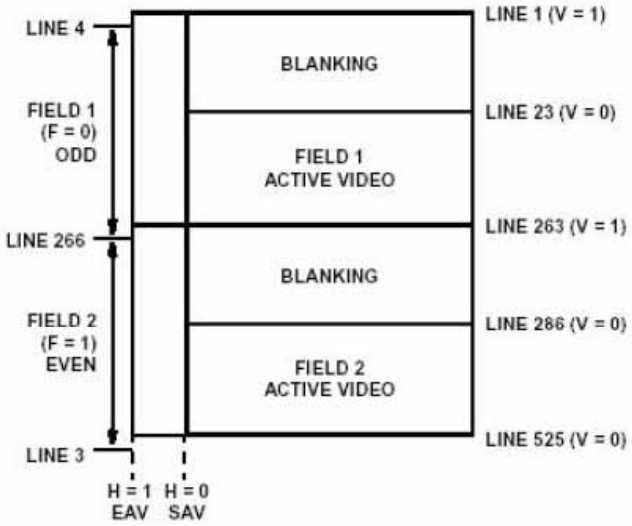
Table 65. CCIR_656 XY Table

XY							
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
1	F	V	H	P3	P2	P1	P0

- Control is provided through "End of Video" (EAV) and "Start of Video" (SAV) timing references.
- Horizontal blanking section consists of repeating pattern 80 10 80 10

14.11. CCIR656 vertical input timing

14.11.1. NTSC mode

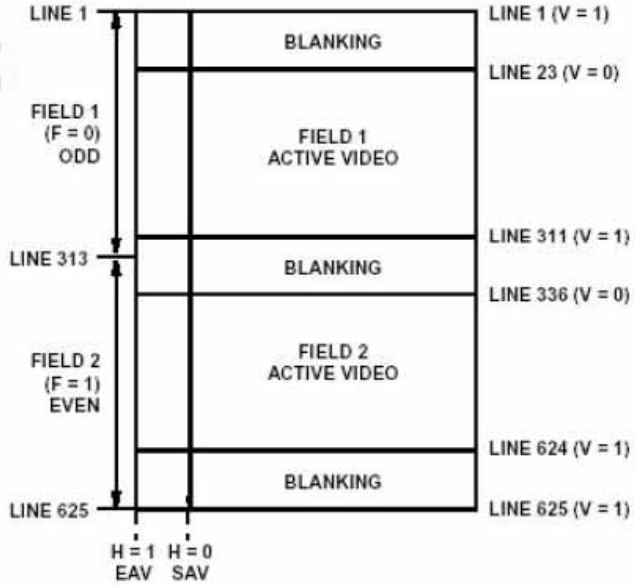


LINE NUMBER	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-22	0	1	1	0
23-262	0	0	1	0
263-265	0	1	1	0
266-285	1	1	1	0
286-525	1	0	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	ODD Field	SAV	ACTIVE VIDEO

Figure 33. CCIR656 NTSC Timing Chart

14.11.2. PAL mode



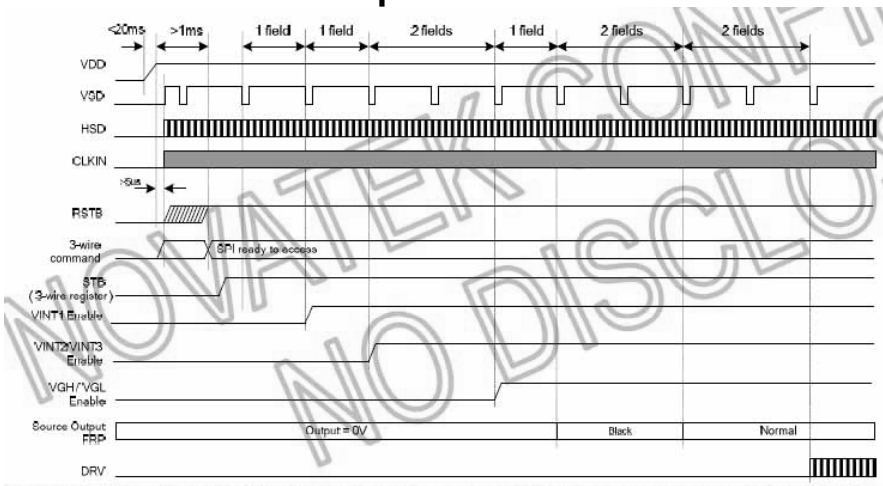
LINE NUMBER	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	ODD Field	SAV	ACTIVE VIDEO

Figure 34. CCIR656 PAL Timing Chart

1.7 Power ON/OFF SEQUENCE

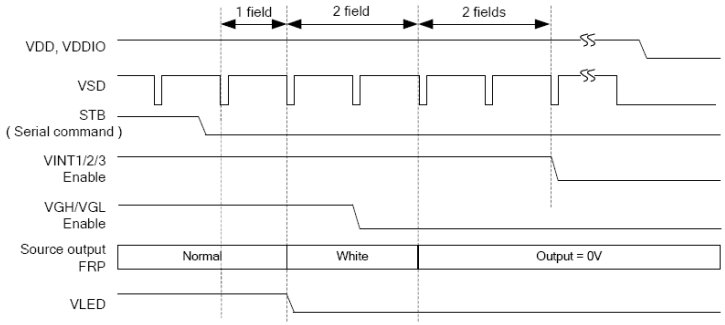
1.7.1 Power ON Sequence



Note: 1. The RSTB should keep low state till VDD was stable, and set to high state before SPI command start.
2. After STB set to 1, it takes 9 VSD period for power on operation.

Figure 17. Power On Sequence Diagram

1.7.2 Power OFF Sequence



Note: For properly power off operation, the extra 5 VSD period (or more) after STB set to low were required.

Figure 18. Power Off Sequence Diagram

1.7.3 Standby In Sequence

Standby In (0x2B00)

1.7.4 Standby Out Sequence

Standby Out (0x2B01)

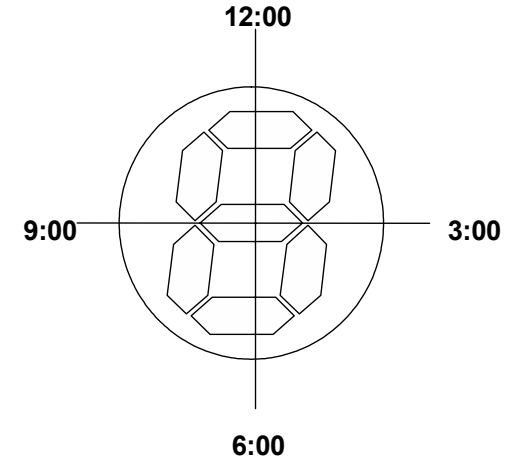
(2) Electro-optical Units

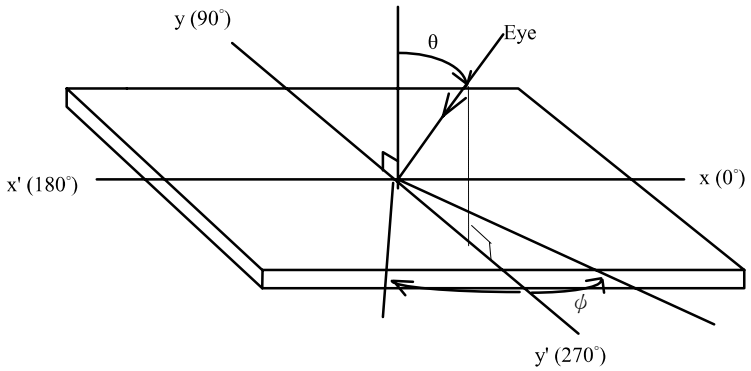
2.1 Electro-optical Characteristics

ITEM	SYMBOL		CONDITION	MIN.	TYP.	MAX.	UNIT
View Angle (Transmissive)	ψ= 90° (12H)		CR>=10	15	20	-	deg.
	ψ= 270° (6H)			50	55	-	deg.
	ψ= 180° (9H)			45	50	-	deg.
	ψ= 0° (3H)			45	50	-	deg.
Contrast Ratio	CR		Ta=25℃	300	400	-	-
Response Time	Tr+Td		Ta=25℃	-	25	-	ms
Color Coordinate (Transmissive)	White	Wx	Ta=25℃	0.25	0.31	0.37	
		Wy		0.27	0.33	0.39	
LCD Type	TFT , (POSITIVE / Transmissive)						
Viewing Direction	12:00						

Notes：All the optical data should be measured when the display's driven under the TYP. condition.

2.2 Optical Definitions





View Angle

(3) Mechanical Units

3.1 Mechanical Diagram

NO	Document Number	Attachment file
1	DF9624VG-AS1-101	

Double-Click the "Attachment Icon" above for opening attachment file.

3.2 Back-light Specification

LED Backlight Styles:

The LED chips are distributed over the whole light area of the illumination unit, which gives the most uniform light.

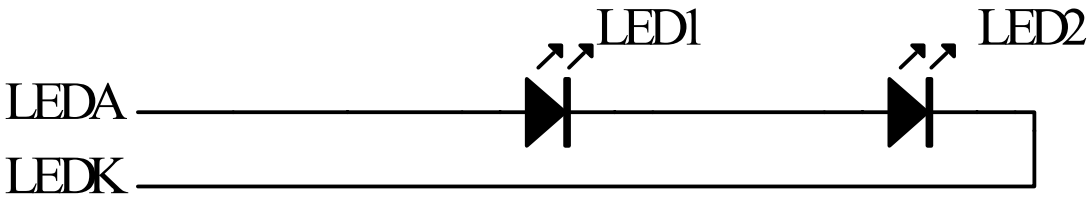
3.2-1. Data About LED Backlight

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	NOTE
Backlight Type	LED / WHITE						-
Supply Current	ILED	-	25	-	mA	VLED<=7.0V	-
Reverse Voltage (Single chip)	VR	-	-	5	V	-	-
Luminous Intensity	IV	250	300	-	cd/m2	-	-
Luminous Intensity Ratio	-			30	%	-	-

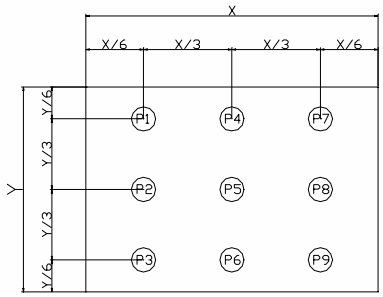
NOTE：1. Average Luminous Intensity of P1 – P9

2. Luminous Intensity Ratio = ((MAX. - MIN.)/ MAX.)*100%

3.2-2. Internal Circuit Diagram



3.2-3. MEASURED METHOD (X*Y: Light Area)



(Effective spatial Distribution)

Hole Diameter φ3mm;1 to 9 per Position Measured Luminous Intensity Ratio

3.3 Packing Method

NO	Document Number	Attachment file
1	DF9624W3-M1-01	

Double-Click the "Attachment Icon" above for opening attachment file.

(4) Quality Units

4.1 Specification of Quality Assurance

4.1-1.Purpose

This standard for Quality Assurance should affirm the quality of LCD module products to supply to purchaser

4.1-2.Standard for Quality Test

a. Inspection :

Before delivering, the supplier should take the following tests, and affirm the quality of product.

b. Electro-Optical Characteristics:

According to the individual specification to test the product.

c. Test of Appearance Characteristics:

According to the individual specification to test the product.

d. Test of Reliability Characteristics:

According to the definition of reliability on the specification for testing products.

e. Delivery Test:

Before delivering, the supplier should take the delivery test.

(i) Test method: According to **ANSI/ASQC Z1.4-2003.General Inspection Level Ⅱ take a single time.**

(ii) The defects classify of AQL as following:

Major defect: AQL=0.65

Minor defect: AQL=2.5

Total defects: AQL=2.5

4.1-3.Nonconforming Analysis & Deal With Manners

a. Nonconforming analysis:

(i) Purchaser should supply the detail data of non-conforming sample and the non-suitable state.

(ii) After accepting the detail data from purchaser, the analysis of nonconforming should be finished in two weeks.

(iii) If supplier can not finish analysis on time, must announce purchaser before two weeks.

b. Disposition of nonconforming:

(i) If find any product defect of supplier during assembly time, supplier must change the good product for every defect after recognition.

(ii) Both supplier and customer should analyze the reason and discuss the disposition of nonconforming when the reason of nonconforming is not sure.

4.1-4. Agreement items

Both sides should discuss together when the following problems happen.

a. There is any problem of standard of quality assurance, and both sides think that it must be modified.

b. There is any argument item which does not record in the standard of quality assurance.

c. Any other special problem.

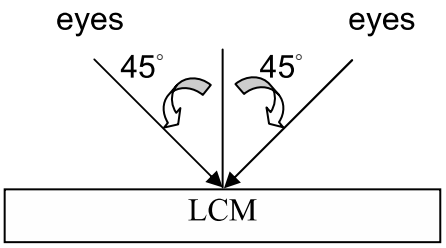
4.1-5. Standard of The Product Appearance Test

a. Manner of appearance test:

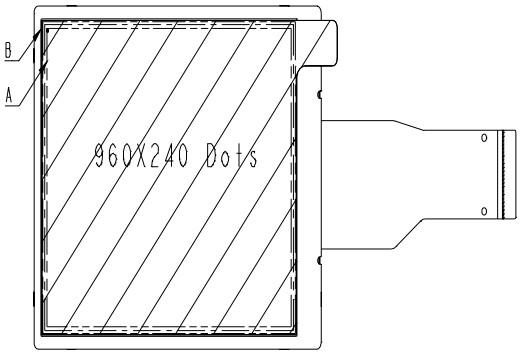
(i) The test must be under 20W × 2 or 40W fluorescent light, and the distance of view must be at 30 cm.

(ii) When display on use front-light test, while display off use back-light test.

(iii)The test direction is base on about around 45° of vertical line.



(iv) Definition of area:



A Area : Viewing area.

B Area : Out of viewing area (Outside viewing area)

Any defect at area B could be ignored. If customer has particular requirement, this requirement should be clearly defined in inspection specification. If inspection specification has defined other criteria, the final judgement should follow the inspection specification .

b. Basic principle:

(i) It will accord to the AQL when the standard can not be described.

(ii) The sample of the lowest acceptable quality level must be discussed by both supplier and customer when any dispute happened.

(iii) Must add new item on time when it is necessary.

c. Standard of inspection:(Unit: mm)

4.1-6. Inspection specification

NO	Document Number	Attachment file
1	M1L070012	

Double-Click the "Attachment Icon" above for opening attachment file.

4.2 Standard Specification for Reliability

NO	Document Number	Attachment file
1	M3ET090005	

Double-Click the "Attachment Icon" above for opening attachment file.

4.3 Precautions in Use of LCM

4.3-1 Handling of LCM

- Don't give external shock.
- Don't apply excessive force on the surface.
- Liquid in LCD is hazardous substance. Must not lick and swallow. when the liquid is attach to your hand, skin, cloth etc. Wash it out thoroughly and immediately.
- Don't operate it above the absolute maximum rating.
- Don't disassemble the LCM.

4.3-2 Storage

- Store in an ambient temperature of 5℃ to 45℃, and in a relative humidity of 40% to 60%. Don't expose to sunlight or fluorescent light.
- Storage in a clean environment, free from dust, active gas, and solvent.
- Store in anti-static electricity container.
- Store without any physical load.

4.3-3 Soldering

- Use the Sn-Ag-Cu (96.5, 3.0, 0.5) solder
- Iron : Temperature 300℃ and less than 5-6 sec during soldering.
- Rewiring : no more than 3 times.

4.3-4 Assembly

- The front polarizer is covered with a protective foil which should be removed before use.

(5) Substance Management Units

5.1 Product Substances Management Documentation

NO	Document Number	Attachment file
1	Environment management standard(EMS-P-017-01)	

Double-Click the "Attachment Icon" above for opening attachment file.