

Product Specifications

Model Name	S028HQ29NN
Description	240(RGB)x320 Dots 2.8" TFT LCD
Date	2019/04/11
Revision	2.0

Customer Approval

Customer Approval	
Date	

Engineering

Check	Date	Prepared	Date
ZHP	2018/11/22	Yigui.Han	2018/11/22

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2 General Specifications

Feature		Spec
Characteristics	Size	2.8inch
	Resolution	240(horizontal)*320(Vertical)
	Interface	MCU-18/16/9/8 Bit RGB-18/16/6 Bit SPI 3-Line&4-Line
	Connect type	Connector
	Color Depth	262k
	Technology type	a-Si
	Display Spec. Pixel pitch (mm)	0.18 x 0.18
	Pixel Configuration	R.G.B. Vertical Stripe
	Display Mode	Normally Black
	Driver IC	ILI9340X
	Viewing Direction	Full view
Mechanical	LCM (W x H x D) (mm)	50.2*69.2*2.75
	Active Area(mm)	43.2*57.6
	Weight (g)	TBD
	LED Numbers	4 LEDs

Note 1: RoHS

Note 2: LCM weight tolerance: +/- 5%

3 Input/Output Terminals

No.	Symbol	Description																																																																																													
1	LEDK	LED Cathode K																																																																																													
2	LEDA1	LED Anode A1																																																																																													
3	LEDA2	LED Anode A2																																																																																													
4	LEDA3	LED Anode A3																																																																																													
5	LEDA4	LED Anode A4																																																																																													
6	IM0	<table border="1"> <thead> <tr> <th rowspan="2">IM3</th> <th rowspan="2">IM2</th> <th rowspan="2">IM1</th> <th rowspan="2">IM0</th> <th rowspan="2">MCU-Interface Mode</th> <th colspan="2">Pins in use</th> </tr> <tr> <th>Register/Content</th> <th>GRAM</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>8080 MCU 8-bit bus interface I</td> <td>D[7:0]</td> <td>D[7:0], WRX, RDX, CSX, D/CX</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>8080 MCU 16-bit bus interface I</td> <td>D[7:0]</td> <td>D[15:0], WRX, RDX, CSX, D/CX</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>8080 MCU 9-bit bus interface I</td> <td>D[7:0]</td> <td>D[8:0], WRX, RDX, CSX, D/CX</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>8080 MCU 18-bit bus interface I</td> <td>D[7:0]</td> <td>D[17:0], WRX, RDX, CSX, D/CX</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>3-wire 9-bit data serial interface I</td> <td colspan="2">SCL, SDA, CSX</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>4-wire 8-bit data serial interface I</td> <td colspan="2">SCL, SDA, D/CX, CSX</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>8080 MCU 16-bit bus interface II</td> <td>D[8:1]</td> <td>D[17:10], D[8:1], WRX, RDX, CSX, D/CX</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>8080 MCU 8-bit bus interface II</td> <td>D[17:10]</td> <td>D[17:10], WRX, RDX, CSX, D/CX</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>8080 MCU 18-bit bus interface II</td> <td>D[8:1]</td> <td>D[17:0], WRX, RDX, CSX, D/CX</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>8080 MCU 9-bit bus interface II</td> <td>D[17:10]</td> <td>D[17:9], WRX, RDX, CSX, D/CX</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>3-wire 9-bit data serial interface II</td> <td colspan="2">SCL, SDI, SDO, CSX</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>4-wire 8-bit data serial interface II</td> <td colspan="2">SCL, SDI, D/CX, SDO, CSX</td> </tr> </tbody> </table>	IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use		Register/Content	GRAM	0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0], WRX, RDX, CSX, D/CX	0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0], WRX, RDX, CSX, D/CX	0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0], WRX, RDX, CSX, D/CX	0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0], WRX, RDX, CSX, D/CX	0	1	0	1	3-wire 9-bit data serial interface I	SCL, SDA, CSX		0	1	1	0	4-wire 8-bit data serial interface I	SCL, SDA, D/CX, CSX		1	0	0	0	8080 MCU 16-bit bus interface II	D[8:1]	D[17:10], D[8:1], WRX, RDX, CSX, D/CX	1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10], WRX, RDX, CSX, D/CX	1	0	1	0	8080 MCU 18-bit bus interface II	D[8:1]	D[17:0], WRX, RDX, CSX, D/CX	1	0	1	1	8080 MCU 9-bit bus interface II	D[17:10]	D[17:9], WRX, RDX, CSX, D/CX	1	1	0	1	3-wire 9-bit data serial interface II	SCL, SDI, SDO, CSX		1	1	1	0	4-wire 8-bit data serial interface II	SCL, SDI, D/CX, SDO, CSX	
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7	IM1																																																																																														
8	IM2																																																																																														
9	IM3																																																																																														
10	RESET	Reset signal pin																																																																																													
11	VSYNC	Frame Synchronous Signal																																																																																													
12	HSYNC	Line Synchronous Signal																																																																																													
13	DOTCLK	Dot-clock signal and oscillator source																																																																																													
14	DE	Display enable signal																																																																																													
15~32	DB17~ DB0	Data bus DB17~ DB0																																																																																													
33	SDO	Serial output signal																																																																																													
34	SDI	Serial input signal																																																																																													
35	RD	Read signal pin																																																																																													
36	WRX/DCX	8080-I system :Write signal Serial interface: Data or command select.																																																																																													
37	DCX/SCL	8081-I system :Data or command select. Serial interface:Serial clock signal.																																																																																													
38	CSX	Chip select pin																																																																																													
39	TE	FMARK																																																																																													
40	VDDI	Interface I/O Power supply (1.65~3.3V)																																																																																													
41	VDDI																																																																																														
42	VCI	Power supply of the System(2.8V)																																																																																													
43	GND	Power Ground																																																																																													
44	X+/XR(NC)	No connection																																																																																													

45	Y+/YD(NC)	No connection
46	X-/XL(NC)	No connection
47	Y-/YU(NC)	No connection
48	GND	Power Ground
49	GND	Power Ground
50	GND	Power Ground

4 Absolute Maximum Ratings

Driving TFT LCD Panel

Item	Symbol	MIN	MAX	Unit	Remark
Supply Voltage	V _{CC}	-0.3	4.6	V	
Operating Temperature	T _{OPR}	-20	60	°C	
Storage Temperature	T _{STG}	-30	70	°C	

5 Electrical Characteristics

5.1 Driving TFT LCD Panel

T_a = 25 °C

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Digital Supply Voltage	V _{CC}	2.5	2.8	3.3	V	
Operating Current	I _{VCC}	-	8.0	-	mA	
Sleeping Current	I _{ST}	-	200	-	uA	
Input Signal Voltage	Low Level	V _{IL}	-0.3	-	0.2x IOVCC	V
	High Level	V _{IH}	0.8x IOVCC	-	IOVCC	V
TFT Common Electrode	V _{COMH}	3	5	5	V	
TFT Gata ON Voltage	V _{GH}	10	-	16	V	
TFT Gata ON Voltage	V _{GL}	-10	-	-5	V	

5.2 Driving Backlight

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I _F	-	80	-	mA	Constant current
Forward Voltage	V _F	3	3.2	3.4	V	
Backlight Power consumption	W _{BL}	-	0.256	-	W	

LED Lifetime		-	25000	-	Hrs	
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Note : Each LED : IF =20 mA, VF =3.2V.

Note 2: Optical performance should be evaluated at Ta=25°C only.

Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

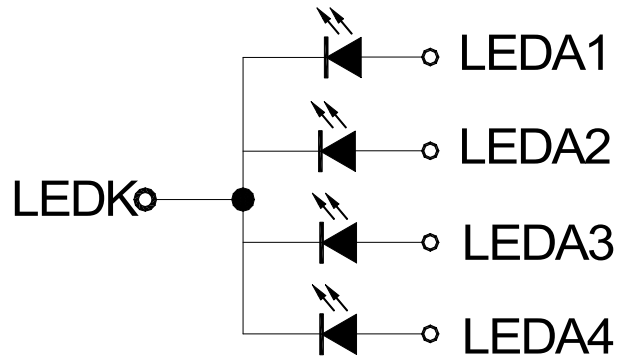
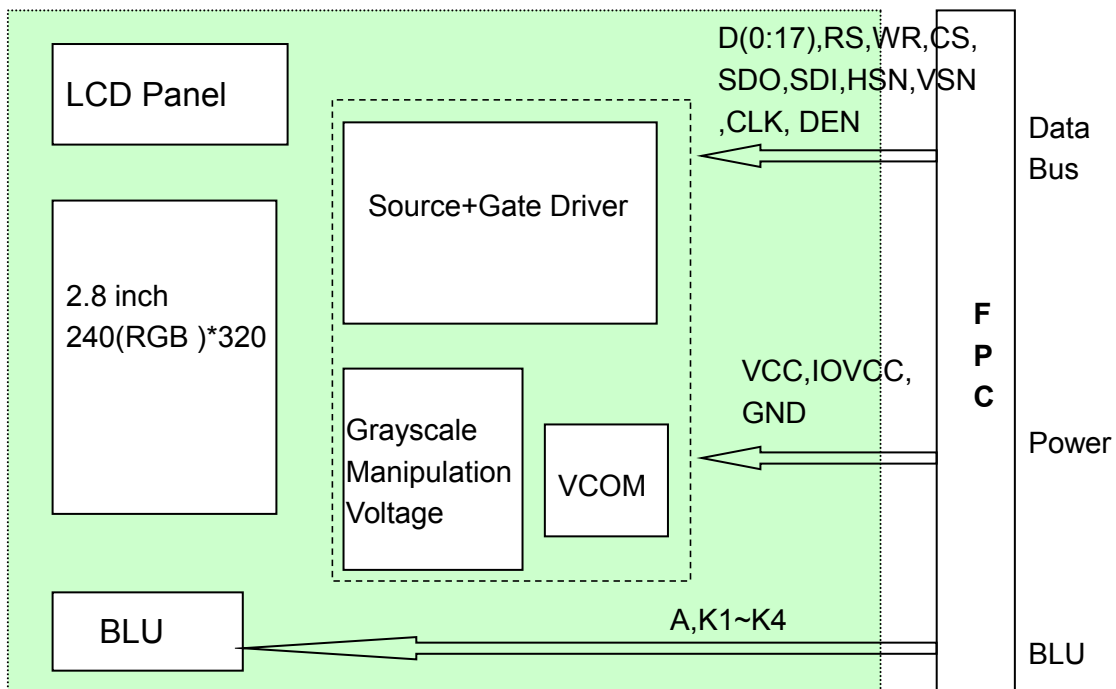


Figure : LED connection of backlight

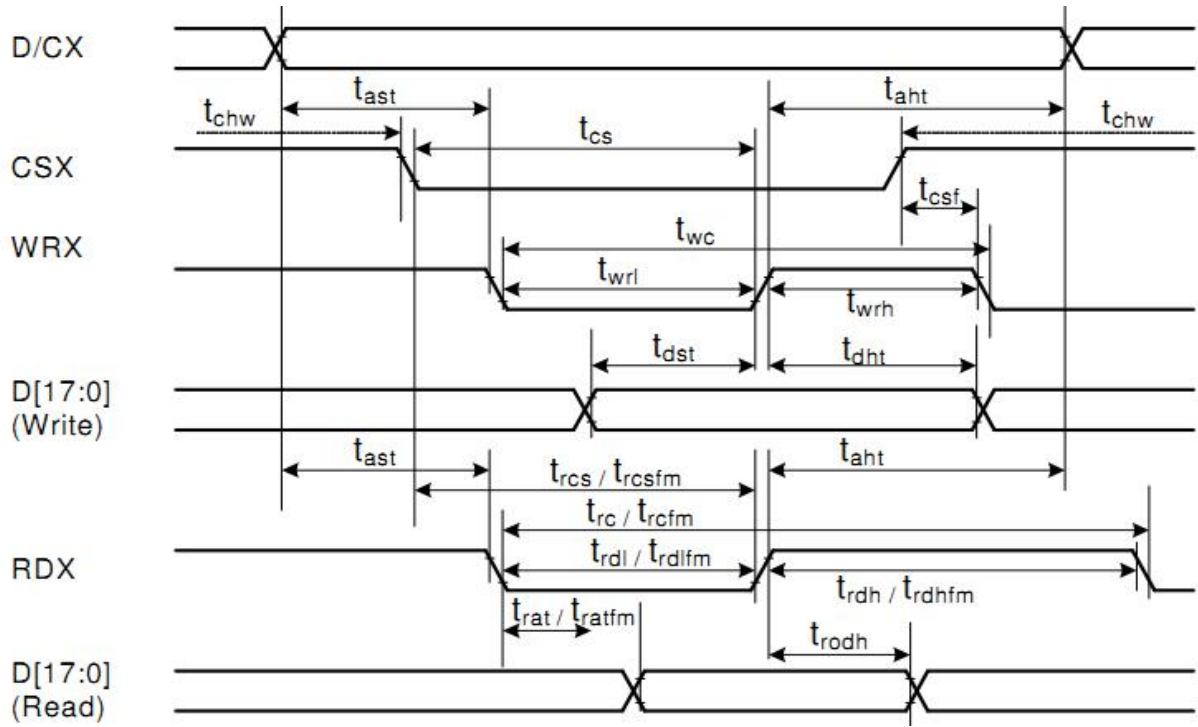
5.3 Block Diagram



6 Interface Timing

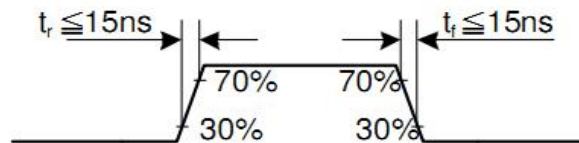
6.1 Timing Parameter

6.1.1 Parallel 18/16/9/8 bit interface timing(8080-II system)

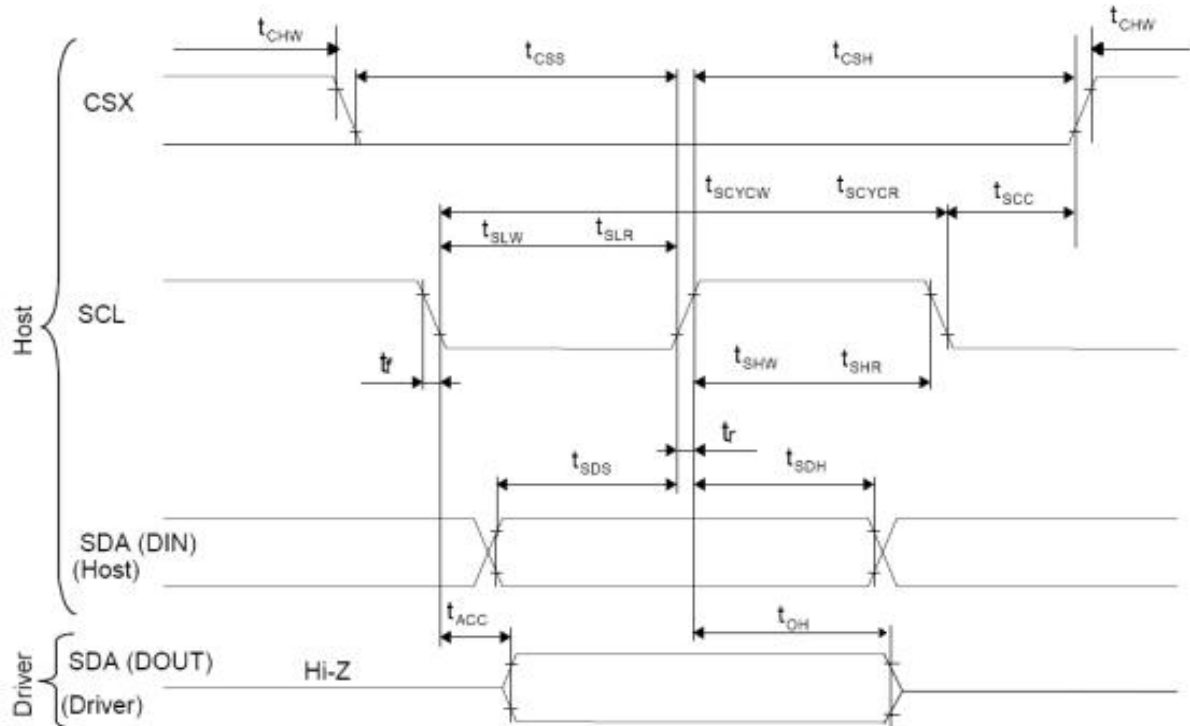


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: $T_a = -30$ to 70 °C, $V_{DDI}=1.65V$ to $3.3V$, $V_{CI}=2.5V$ to $3.3V$, $V_{SS}=0V$.

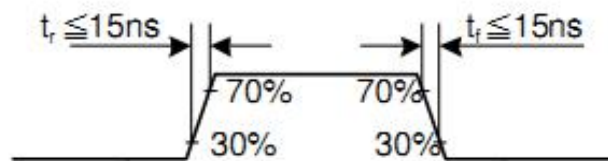


6.1.2 Serial interface timing characteristics (3-line SPI system)

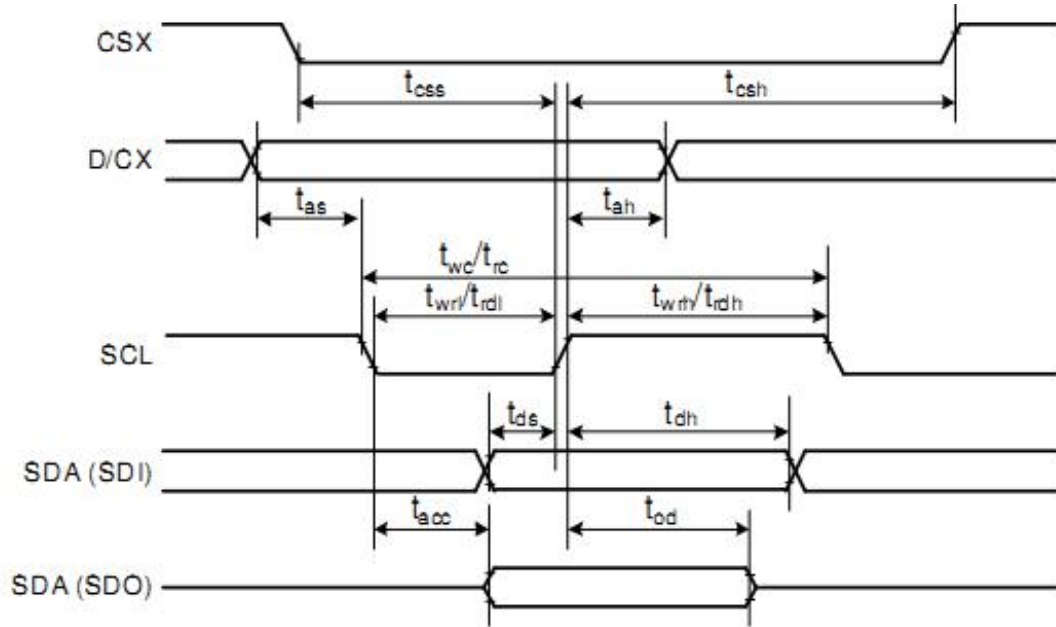


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscyrcr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tsc	SCL-CSX	20	-	ns	
	tch	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
			65	-	ns	

Note: $T_a = 25\text{ }^\circ\text{C}$, $V_{DDI} = 1.65\text{V to }3.3\text{V}$, $V_{CI} = 2.5\text{V to }3.3\text{V}$, $AGND = VSS = 0\text{V}$

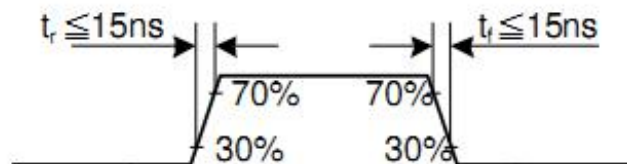


6.1.3 Serial interface timing characteristics (4-line SPI system)

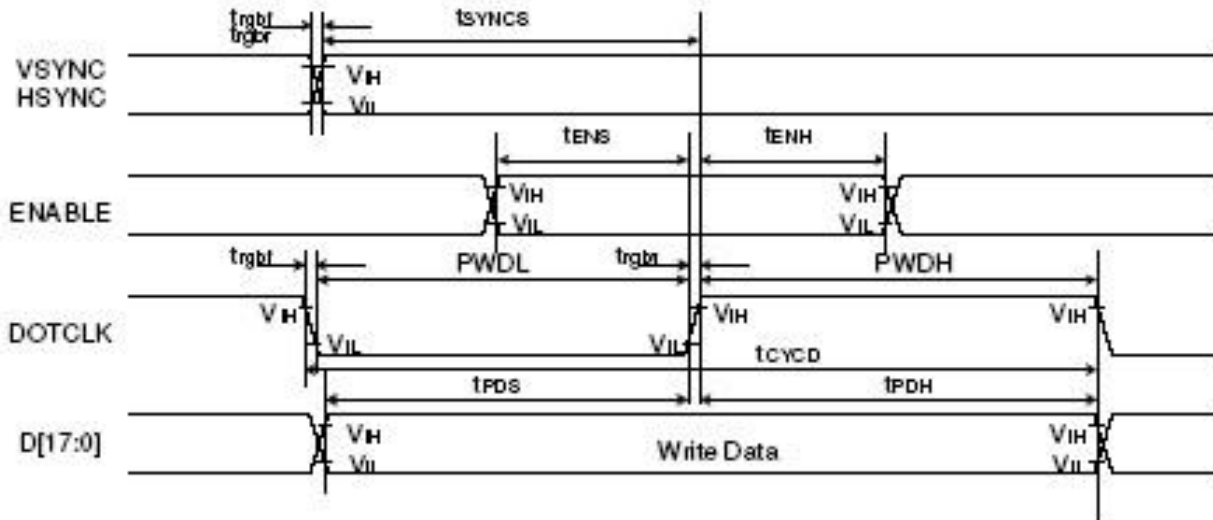


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	t_{css}	Chip select time (Write)	40	-	ns	
	t_{csh}	Chip select hold time (Read)	40	-	ns	
SCL	t_{wc}	Serial clock cycle (Write)	100	-	ns	
	t_{wrh}	SCL "H" pulse width (Write)	40	-	ns	
	t_{wrl}	SCL "L" pulse width (Write)	40	-	ns	
	t_{rc}	Serial clock cycle (Read)	150	-	ns	
	t_{rdh}	SCL "H" pulse width (Read)	60	-	ns	
	t_{rdl}	SCL "L" pulse width (Read)	60	-	ns	
D/CX	t_{as}	D/CX setup time	10	-		
	t_{ah}	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	t_{ds}	Data setup time (Write)	30	-	ns	
	t_{dh}	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	t_{acc}	Access time (Read)	10	-	ns	For maximum $C_L=30\text{pF}$
	t_{od}	Output disable time (Read)	10	50	ns	For minimum $C_L=8\text{pF}$

Note: $T_a = 25^\circ\text{C}$, $V_{DDI}=1.65\text{V to }3.3\text{V}$, $V_{CI}=2.5\text{V to }3.3\text{V}$, $AGND=VSS=0\text{V}$

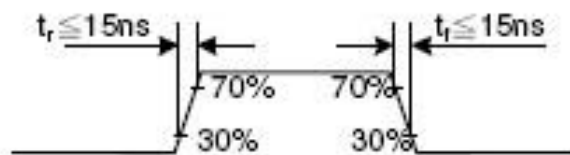


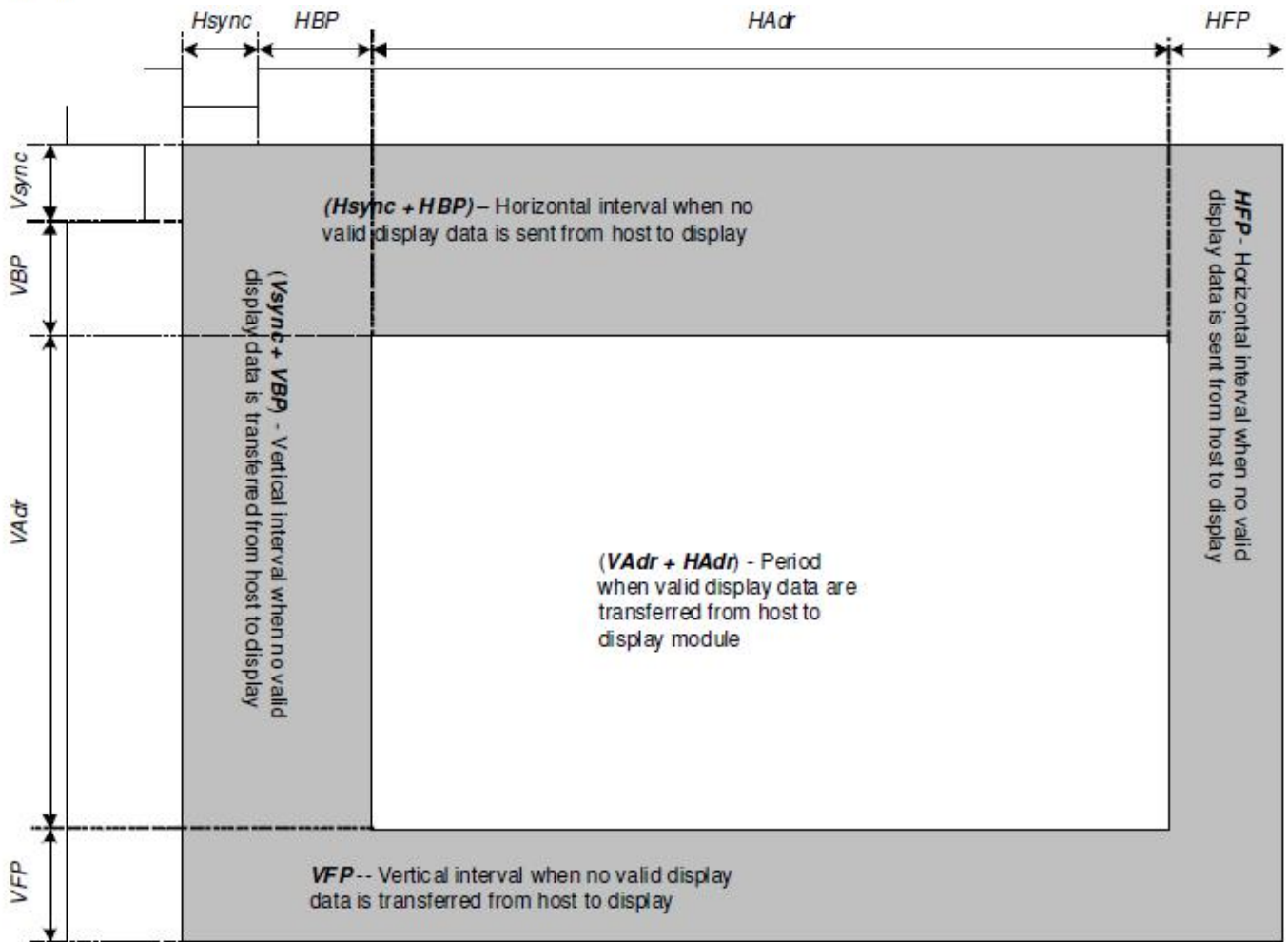
6.1.4 Parallel 18/16/9/8 bit RGB interface timing



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/ HSYNC	t_{synCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{synCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{deS}	DE setup time	15	-	ns	
	t_{deH}	DE hold time	15	-	ns	
D[17:0]	t_{Dcs}	Data setup time	15	-	ns	
	t_{Dch}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rtr}, t_{ftf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC/ HSYNC	t_{synCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{synCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{deS}	DE setup time	15	-	ns	
	t_{deH}	DE hold time	15	-	ns	
D[17:0]	t_{Dcs}	Data setup time	15	-	ns	
	t_{Dch}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rtr}, t_{ftf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: $T_a = -30$ to 70 °C, $V_{DDI} = 1.85V$ to $3.3V$, $V_{CI} = 2.5V$ to $3.3V$, $AGND = VSS = 0V$

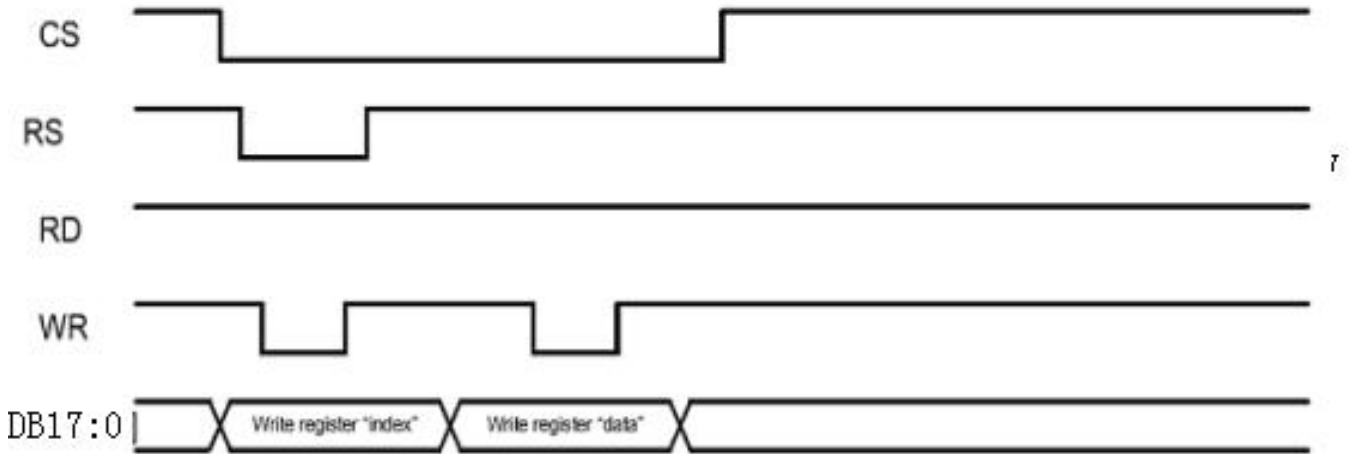




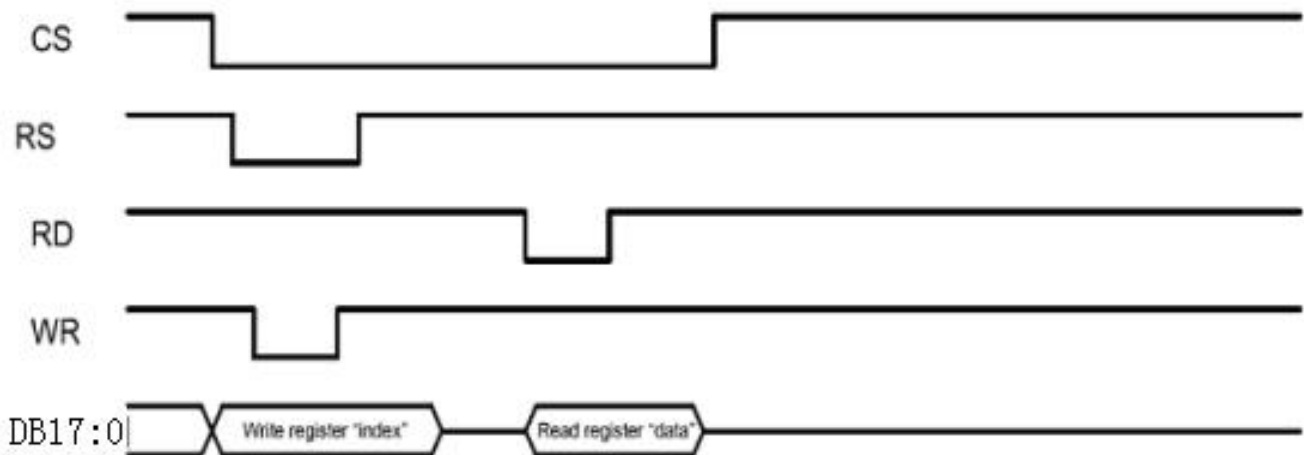
Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line

6.2 Register Write/Read Timing

(a) Write to register

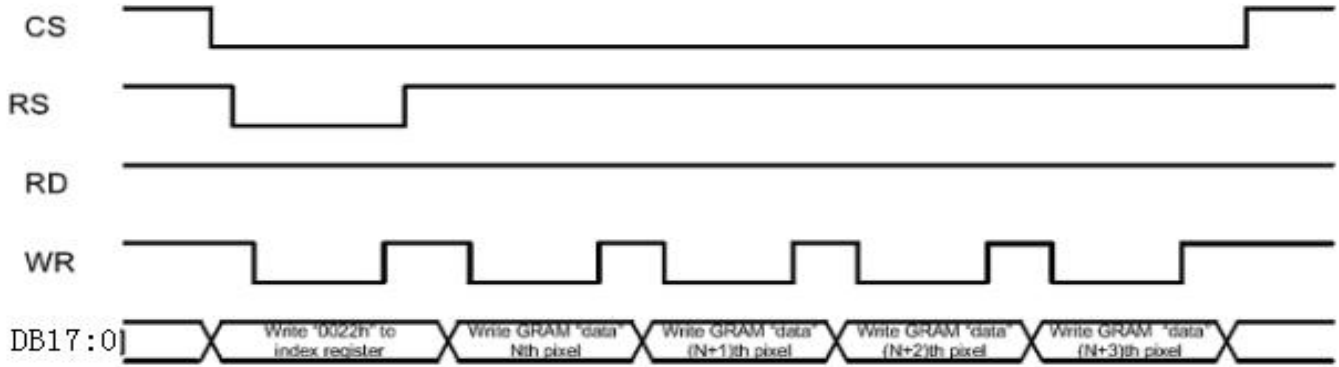


(b) Read from register

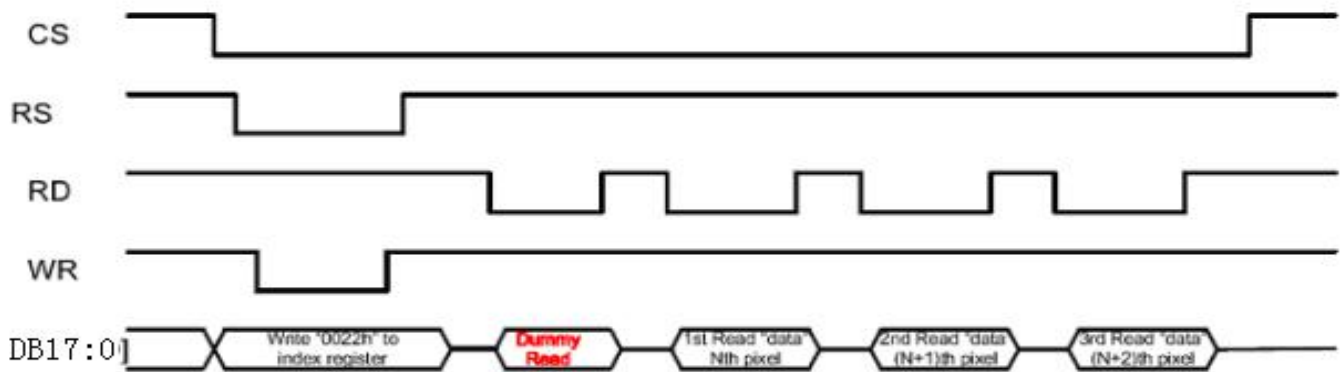


6.3 GRAM Wite/Read Timing

(a) Write to GRAM

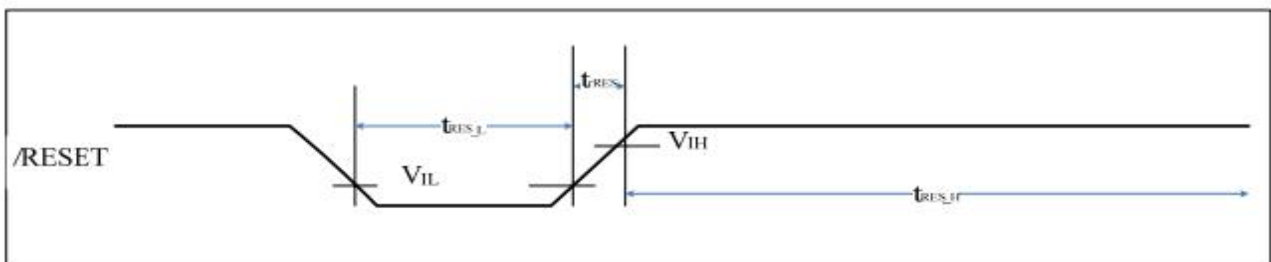


(b) Read from GRAM



6.4 Reset Timing Characteristics

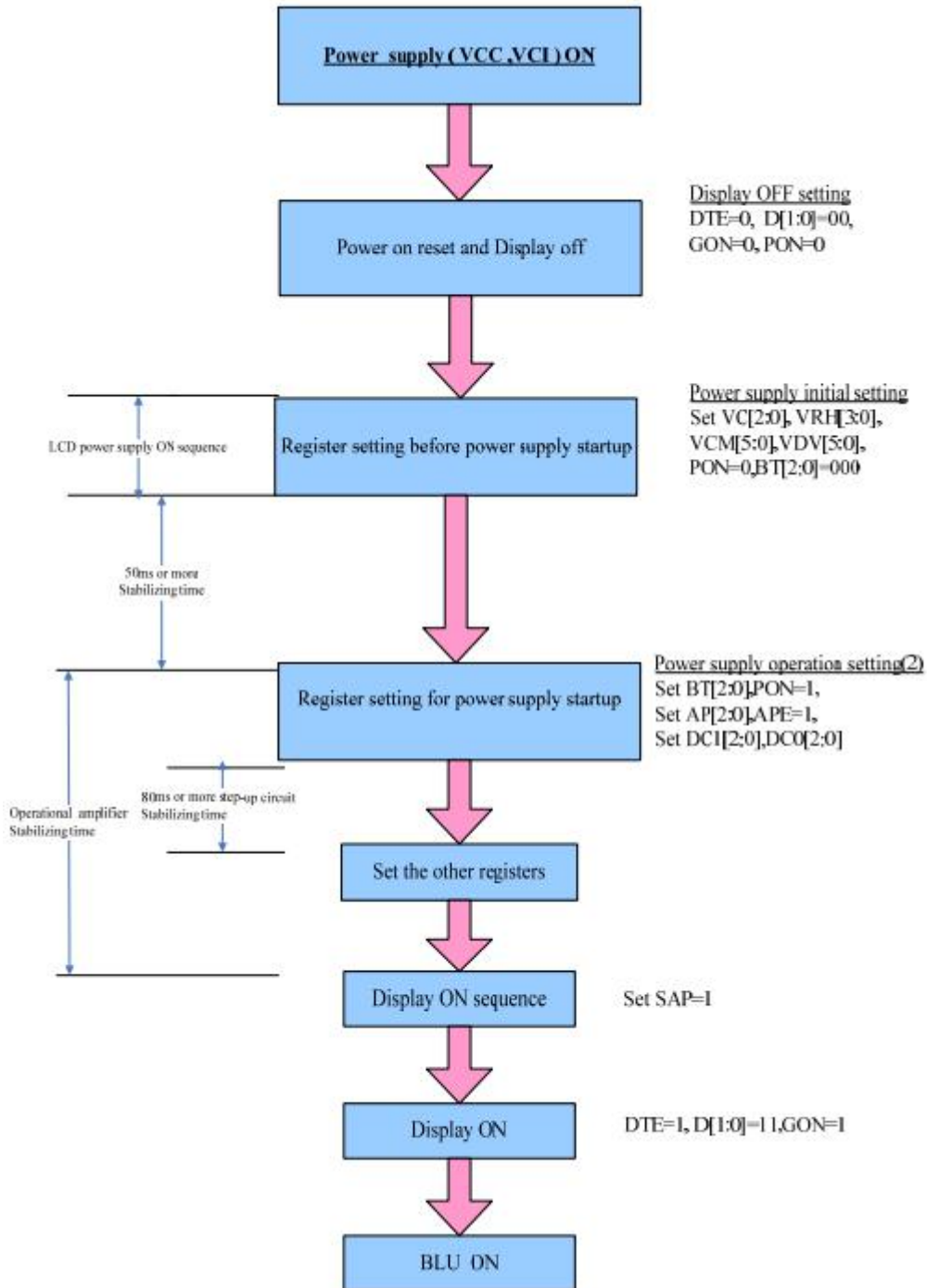
Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	t_{RESL}	ms	1	-	-
Reset rise time	t_{RES}	μs	-	-	10
Reset high-level width	t_{RESH}	ms	50		



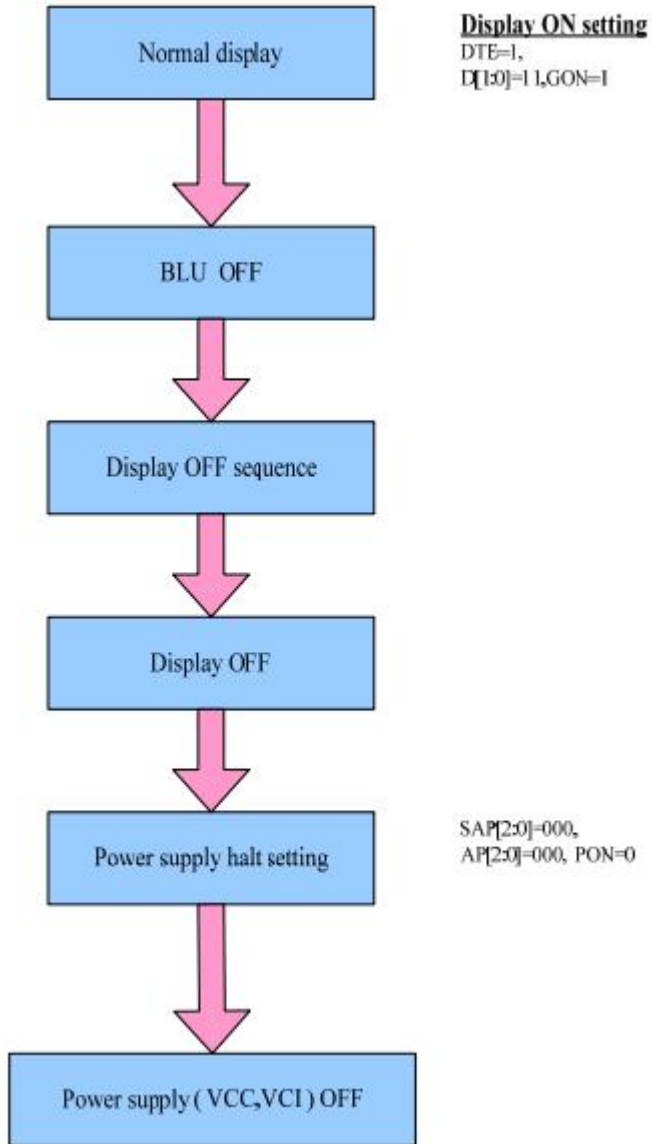
Reset timing

6.5 Power On/Off Sequence

6.5.1 Power On Sequence



6.5.2 Power Off Sequence



7 Optical Characteristics

Items	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	
Viewing angles	θ_T	Center $CR \geq 10$	-	80	-	Degree.	Note2	
	θ_B		-	80	-			
	θ_L		-	80	-			
	θ_R		-	80	-			
Contrast Ratio	CR	$\Theta = 0$	400	500	-	-	Note1, Note3	
Surface luminance	LV	$\theta = 0^\circ$	300	350	-	cd/m ²	Note2	
Response Time	T_{ON}	25° C	-	30	40	ms	Note1, Note4	
	T_{OFF}		-	30	40			
Chromaticity	White	Backlight is on	X_W	TBD	TBD	TBD	-	Note1, Note5
			Y_W	TBD	TBD	TBD	-	
	Red		X_R	TBD	TBD	TBD	-	
			Y_R	TBD	TBD	TBD	-	
	Green		X_G	TBD	TBD	TBD	-	
			Y_G	TBD	TBD	TBD	-	
	Blue		X_B	TBD	TBD	TBD	-	
			Y_B	TBD	TBD	TBD	-	
Uniformity	U		75	80	-	%	Note1, Note6	
NTSC				65		%	Note5	
Luminance	L		310	360	400		Note1, Note7	

Test Conditions:

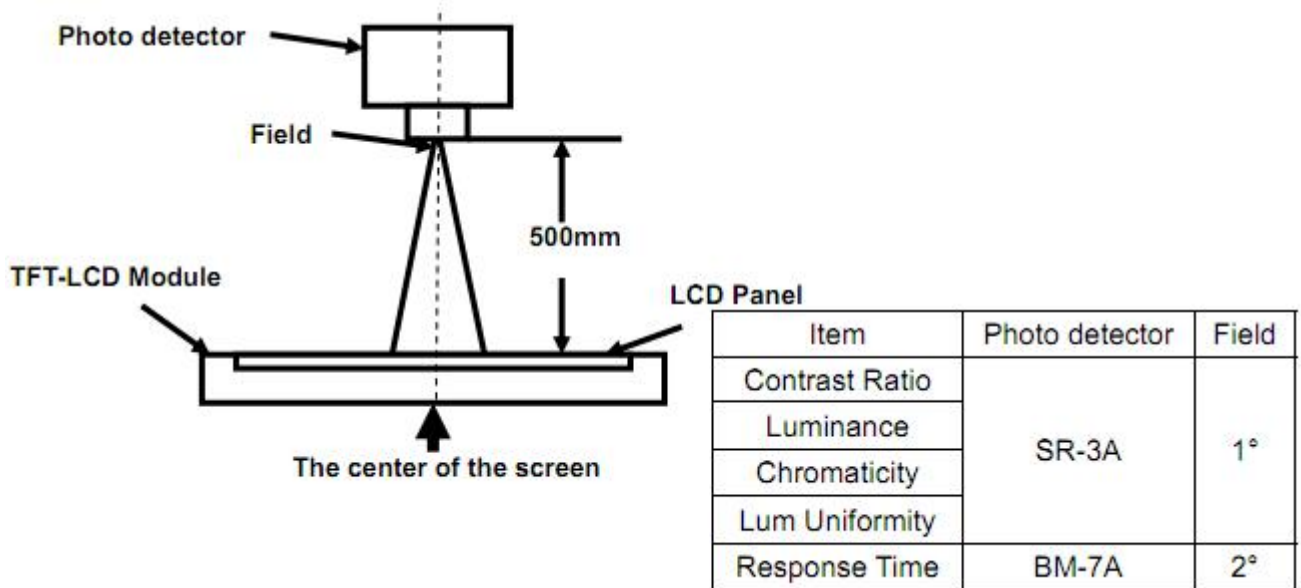
1. IF= 20mA(one channel),the ambient temperature is 25
2. The test systems refer to Note 1 and Note 2.

Note2. Definition of surface luminance.

Surface luminance is the luminance with all pixels displaying white. For more information see
 $L_v = \text{Average Surface Luminance with all white pixels}(P_1, P_2, P_3, \dots, P_n)$

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

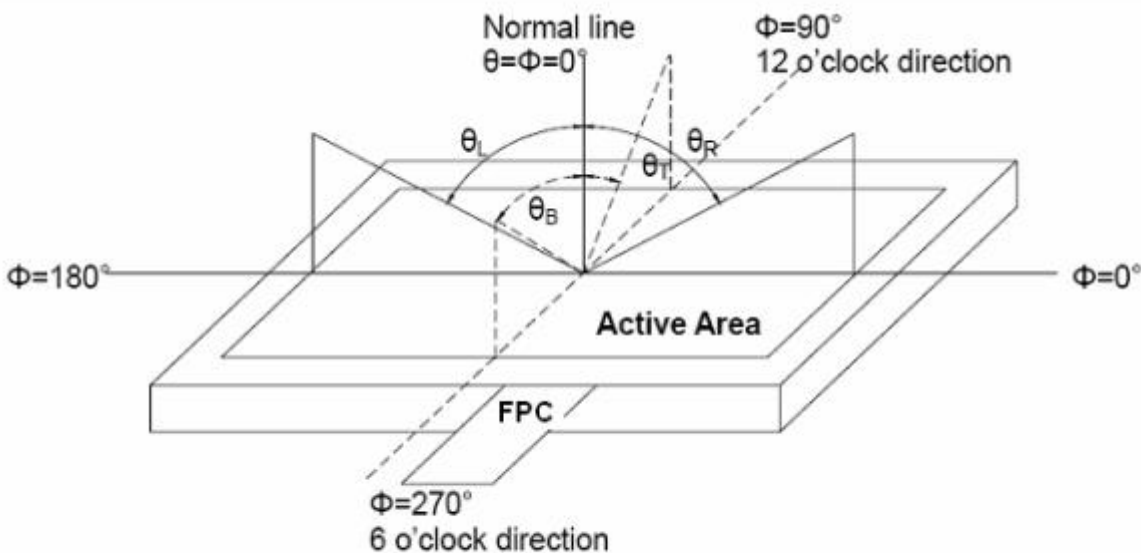


Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

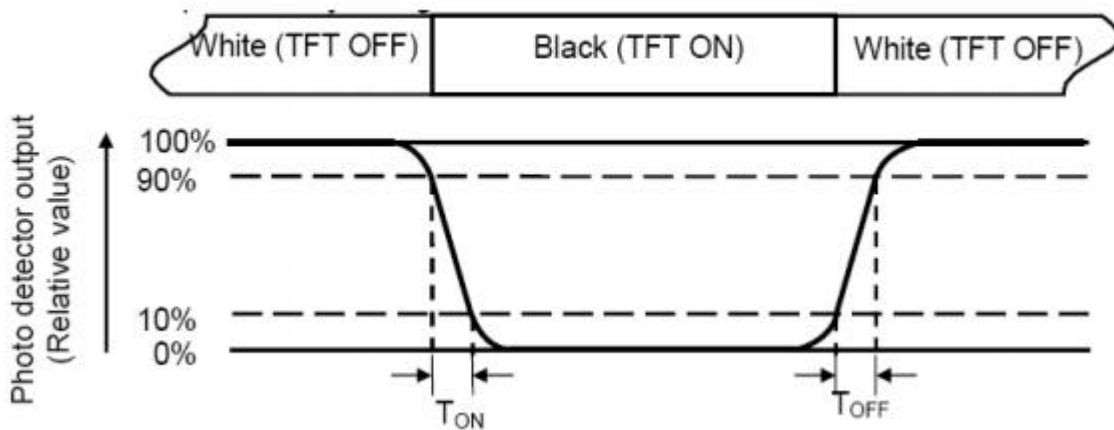
“White state “:The state is that the LCD should driven by V_{white} .

“Black state”: The state is that the LCD should driven by V_{black} .

V_{white} : To be determined V_{black} : To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity}(U) = L_{\min} / L_{\max}$$

L-----Active area length W----- Active area width

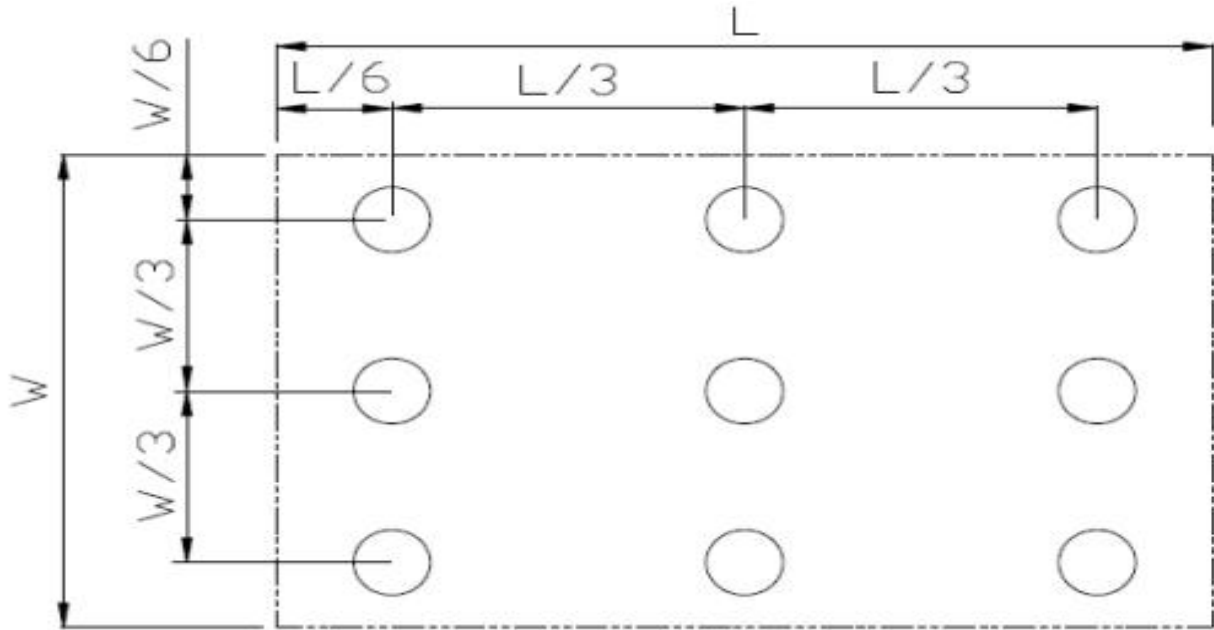


Fig. 2 Definition of uniformity

L_{\max} : The measured maximum luminance of all measurement position.

L_{\min} : The measured minimum luminance of all measurement position.

Note 7: Definition of Luminance :

Measure the luminance of state at point.

8 Environmental / Reliability Tests

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts= +60°C, 120hrs	Note 1 IEC60068-2-2, GB2423. 2-89
2	Low Temperature Operation	Ta= -20°C, 120hrs	Note 2 IEC60068-2-1 GB2423.1-89
3	High Temperature Storage	Ta= +70°C, 240hrs	IEC60068-2-2 GB2423. 2-89
4	Low Temperature Storage	Ta= -30°C, 240hrs	IEC60068-2-1 GB/T2423.1-89
5	High Temperature & Humidity Storage	Ta= +60°C, 90% RH max, 160 hours	IEC60068-2-3 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-30°C 30 min ~ +80°C 30 min Change time: 5min, 30 Cycle	Start with cold temperature, end with high temperature IEC60068-2-14, GB2423.22-87
7	Electro Static Discharge (Operation)	C=150pF, R=330 Ω, 5 points/panel Air: ±8KV, 5 times; Contact: ±4KV, 5 times; (Environment: 15°C ~ 35°C, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2 GB/T17626.2-1998
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (package condition)	IEC60068-2-6 GB/T2423.5-1995
9	Shock (Non-operation)	60G 6ms, ± X, ± Y, ± Z 3 times for each direction	IEC60068-2-27 GB/T2423.5-1995
10	Package Drop Test	Height: 80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8-1995

Note: 1. Ts is the temperature of panel's surface.

2. Ta is the ambient temperature of sample.



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10 Packing

Packing Method

TBD

11 Precautions For Use of LCD modules

11.1 Handling Precautions

11.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

11.1.6. Do not attempt to disassemble the LCD Module.

11.1.7. If the logic circuit power is off, do not apply the input signals.

11.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

11.1.8.1. Be sure to ground the body when handling the LCD Modules.

11.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

11.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

11.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.2 Storage Precautions

12.2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2. The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0°C ~ 40°C Relatively humidity: ≤80%

11.2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

11.3 Inspection Sampling

3.1. Lot size : Quantity per shipment lot per model

- 3.2. Sampling type: Normal inspection, Single sampling
- 3.3. Inspection level: II
- 3.4. Sampling table : MIL-STD-105D
- 3.5. Acceptable quality level (AQL)
 - Major defect : AQL=0.65
 - Minor defect: AQL=1.00

11.4 Inspection Conditions

4.1 Ambient conditions:

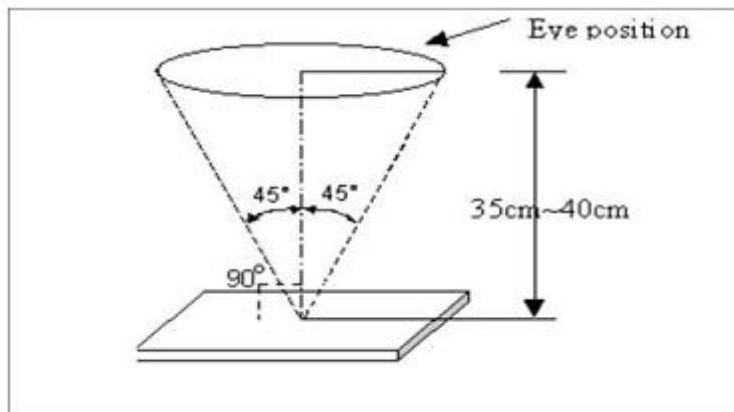
- a. Temperature: Room temperature $25 \pm 5^{\circ}\text{C}$
- b. Humidity: $(60 \pm 10) \% \text{RH}$
- c. Illumination: Single fluorescent lamp non-directive (300 to 700 Lux)

4.2 Viewing distance

The distance between the LCD and the inspector' s eyes shall be at least 35 ± 5 cm.

4.3 Viewing Angle

U/D: 45o/45o, L/R: 45o/45o



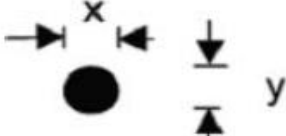
11.5. Inspection Criteria

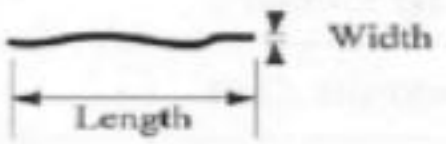
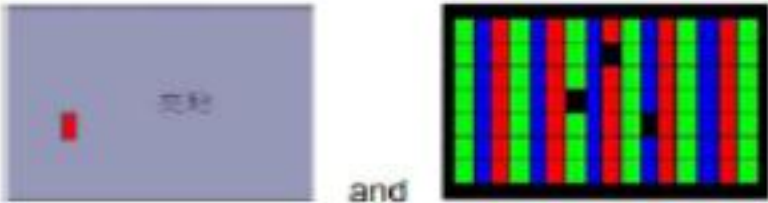
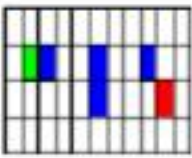
Defects are classified as major defects and minor defects according to the degree of defectiveness defined herein.

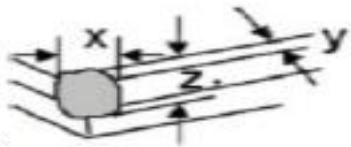

11.5.1 Major defect

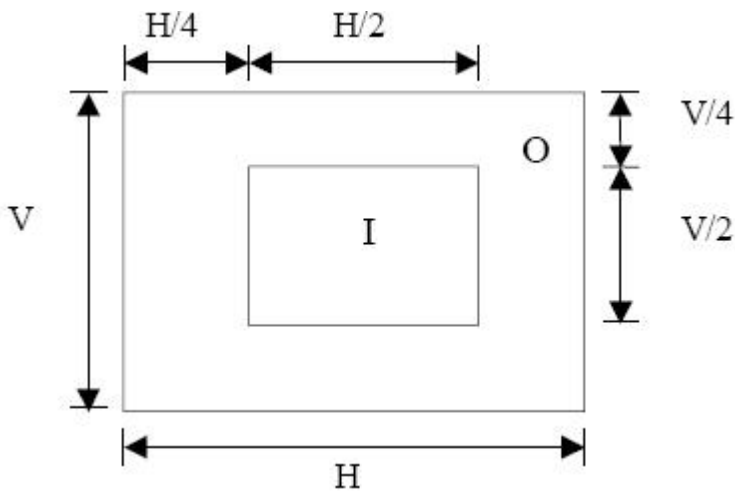
Item No	Items to be inspected	Inspection Standard
5.1.1	All functional defects	1) No display 2) Display abnormally 3) Short circuit 4) line defect
5.1.2	Missing	Missing function component
5.1.3	Crack	Glass Crack

11.5.2 Minor defect

Item No	Items to be inspected	Inspection standard	
5.2.1	Spot Defect Including Black spot White spot Pinhole Foreign particle	For dark/white spot is defined $\varphi = (x+y) / 2$ 	
		Size φ (mm)	Acceptable Quantity
		$\varphi \leq 0.10$	Ignore
		$0.10 < \varphi \leq 0.2$	2
		$0.2 < \varphi$	Not allowed

5.2.2	Polarizer dirt, particle	Size ϕ (mm)	Acceptable Quantity		
		$\phi \leq 0.15$	1		
5.2.3	Line Defect Including Black line White line Scratch	Define:			
					
		Width(mm)	Acceptable Quantity		
		Length(mm)			
		$W \leq 0.05$	Ignore		
		$0.05 < W \leq 0.1$	2		
		$L \leq 1.5$			
		$0.1 < W, \text{ or } L > 1.5$	Not allowed		
5.2.4	Polarizer Dent/Bubble	Not allowed			
5.2.5	Electrical Dot Defect	Bright and Black dot define:			
					
					
		Two Adjacent Dot			
		Inspection pattern: Full white, Full black, Red, green and blue screens			
		Item	Acceptable Quantity		
			I	O	Note
Black dot defect	2		$5\text{mm} \leq \text{Distance}$		
Bright dot defect	1				
Two Adjacent Dot	1				
There or more Adjacent Dot	Not allowed				
Total Dot	2				

5.2.6	Glass defect		
		1. Corner Fragment:	
		Size(mm) $X \leq 2\text{mm}$ $Y \leq 1\text{mm}$ $Z \leq T$	Acceptable Quantity Ignore T : Glass thickness X : Length Y : Width Z : thickness
			
		2. Side Fragment:	
		Size(mm) $X \leq 5.0\text{mm}$ $Y \leq 1\text{mm}$ $Z \leq T$	Acceptable Quantity T : Glass thickness X : Length Y : Width Z : thickness



Note: 1). Dot defect is defined as the defective area of the dot area is larger than 50% of the dot area.

2). The distance between two bright dot defects (red, green, blue, and white) should be larger than 15mm.

3). The distance between black dot defects or black and bright dot defects should be more than 5mm apart.

4). Polarizer bubble is defined as the bubble appears on active display area. The defect of polarizer bubble shall be ignored if the polarizer bubble appears on the outside of active display area.

11.6 Mechanics specification

As for the outside dimension of the modules, please refer to product specification for more details

- Note:
- 1). Dot defect is defined as the defective area of the dot area is larger than 50% of the dot area.
 - 2). The distance between two bright dot defects (red, green, blue, and white)