Model Name: ZXGL65001

LCD Screen model : DV650QUB-P21

DV650QUB-R11

Issue Date : 2023/07/17

( )Preliminary Specifications
(*)Final Specifications

Customer Signature:	
ZXGL Part No.:	
Approved By:	Approval By PM Director
Note:	Reviewed By RD Director
	Reviewed By Project Leader
	Prepared By PM

REVISION HISTORY

Version	Date	Page	Description
1.0	2023/07/17	All	First release

1. GENERAL DESCRIPTION

1.1 OVERVIEW

ZXGL65001 is a color active matrix TFT LCD open cell using amorphous silicon TFT's (Thin Film Transistors) as an active switching device. This module has a 64.5 inch diagonally measured active area with UHD resolutions (3840 horizontal by 2160 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in island and this module can display 1.07G colors. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	65	Inch	-
Driver Element	a-Si TFT active matrix	-	-
Pixel Number	3840 x 2160	Pixel	
Pixel pitch	0.124(H) x 3(RGB)x 0.372 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Display Colors	8bit +FRC / 1.07G	Color	
Transmissive Mode	Normally Black	-	
Surface Treatment	Haze 25%, 3H	-	
Luminance, White	1500~3000	cd/m2	
White luminance uniformity	75	%	
Power Consumption			(1)

Note(1) The specified power consumption: Total=cell(reference 4.3.1)+BL(reference 4.3.2)

2. MECHANICAL SPECIFICATIONS

Item		Min	Typ.	Max	Unit	Note
Module Size	Horizontal(H)		1461		mm	(1)
	Vertical (V)		843.1		mm	
	Thickness (T)		60		mm	
Bezel Area	Horizontal		1431.5		mm	
	Vertical		806.5		mm	
Active Area	Horizontal	-	1428.48	-	mm	
	Vertical	-	803.52	-	mm	
Weight		-	/		Kg	

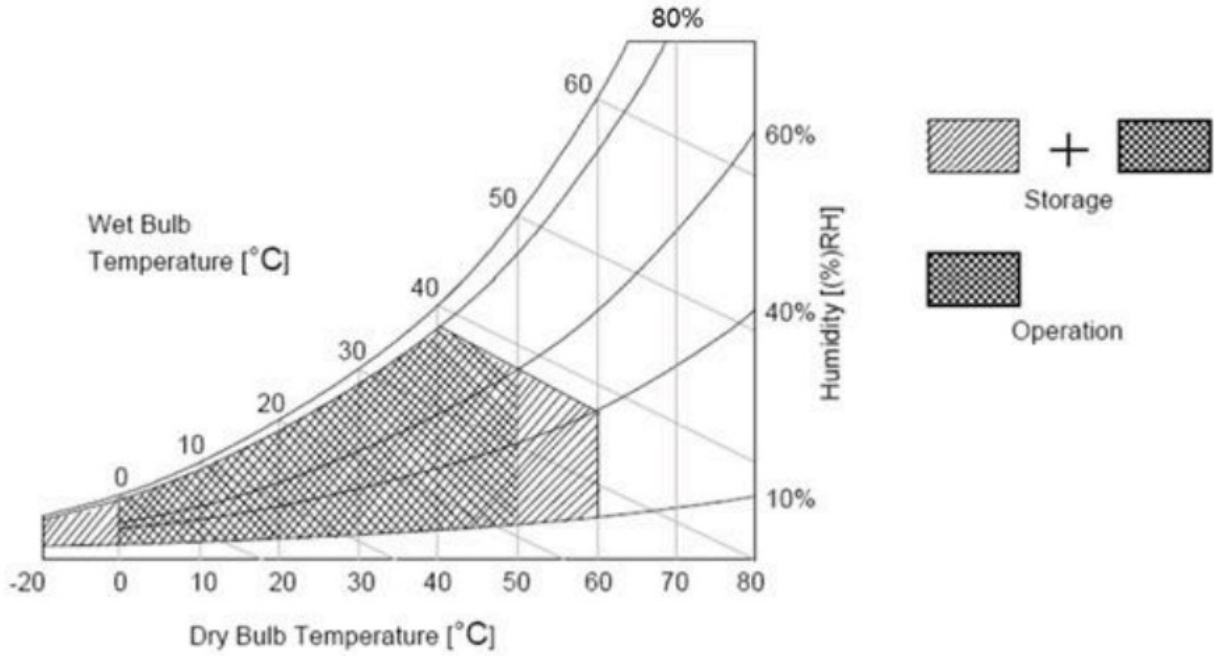
Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

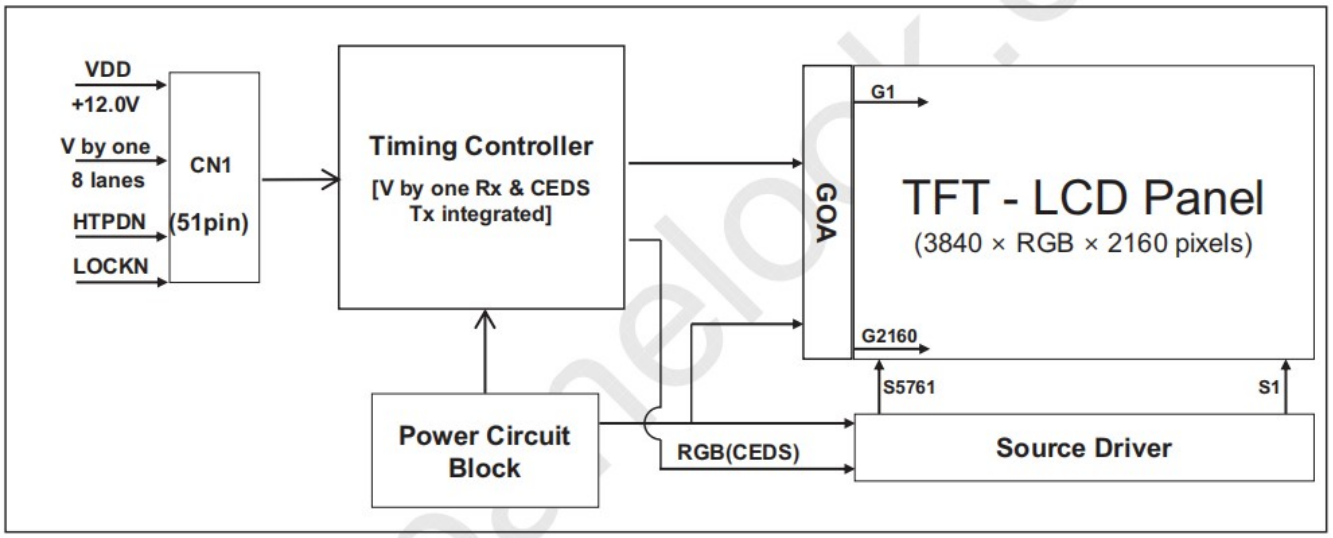
Parameter	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	VSS-0.3	13.2	V	Ta = 25 ℃
Operating Temperature	T_{OP}	0	+50	℃	Note 1
Storage Temperature	T_{SUR}	-20	+60	℃	
	T_{ST}	-20	+60	℃	
Operating Ambient Humidity	Hop	10	80	%RH	
Storage Humidity	Hst	10	80	%RH	

Note 1 : Temperature and relative humidity range are shown in the figure below.
Note 2 : Wet bulb temperature should be 39 ℃ max. and no condensation of water.



4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



- V by one interface with 8 lanes
- High-speed response
- Low color shift image quality
- 8-bit + FRC color depth, display 1.07G colors
- High luminance and contrast ratio, low reflection and wide viewing angle
- Gate driver use GOA mode
- DE (Data Enable) only mode
- ADS technology is applied for high display quality
- RoHS compliant
- Slandscape and Portrait Display
- 7*24hrs in auto aging status

4.2 INTERFACE CONNECTIONS

PIN ASSIGNMENT

V by One CN (51Pin) Connector : F05035-51P-H(CHANGTONG) or Equivalent.

Pin No	Symbol	Description	Pin No	Symbol	Description
1	VDD	Power Supply +12.0V	27	GND	Ground
2	VDD	Power Supply +12.0V	28	Rx0n	V-by-One HS Data Lane 0
3	VDD	Power Supply +12.0V	29	Rx0p	V-by-One HS Data Lane 0
4	VDD	Power Supply +12.0V	30	GND	Ground
5	VDD	Power Supply +12.0V	31	Rx1n	V-by-One HS Data Lane 1
6	VDD	Power Supply +12.0V	32	Rx1p	V-by-One HS Data Lane 1
7	VDD	Power Supply +12.0V	33	GND	Ground
8	VDD	Power Supply +12.0V	34	Rx2n	V-by-One HS Data Lane 2
9	NC	No Connection	35	Rx2p	V-by-One HS Data Lane 2
10	GND	Ground	36	GND	Ground
11	GND	Ground	37	Rx3n	V-by-One HS Data Lane 3
12	GND	Ground	38	Rx3p	V-by-One HS Data Lane 3
13	GND	Ground	39	GND	Ground
14	GND	Ground	40	Rx4n	V-by-One HS Data Lane 4
15	NC	No Connection	41	Rx4p	V-by-One HS Data Lane 4
16	NC	No Connection	42	GND	Ground
17	NC	No Connection	43	Rx5n	V-by-One HS Data Lane 5
18	SDA	SDA	44	Rx5p	V-by-One HS Data Lane 5
19	SCL	SCL	45	GND	Ground
20	NC	No Connection	46	Rx6n	V-by-One HS Data Lane 6
21	NC	No Connection	47	Rx6p	V-by-One HS Data Lane 6
22	SEL_SECTION	Low or NC: 1 section(default) High: 2 section	48	GND	Ground
23	NC	No Connection	49	Rx7n	V-by-One HS Data Lane 7
24	GND	Ground	50	Rx7p	V-by-One HS Data Lane 7
25	HTPDN	Hot plug detect	51	GND	Ground
26	LOCKN	Lock detect			

4.3 ELECTRICAL CHRARCTERISTICS

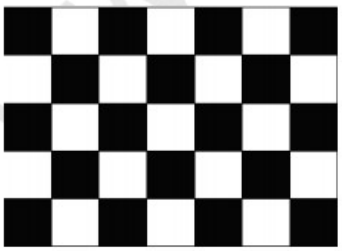
4.3.1 LCD ELETRONICS SPECIFICATION

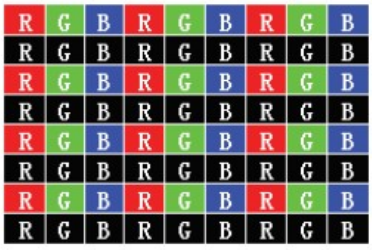
The ambient temperature is Ta = 25 ± 2 °C.

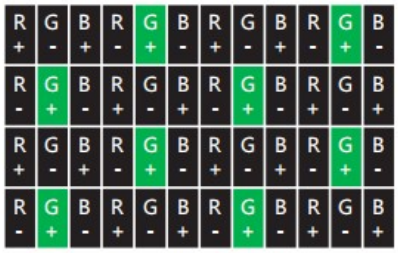
Parameter		Symbol	Values			Unit	Remark
			Min	Typ	Max		
Power Supply Input Voltage		VDD	10.8	12	13.2	Vdc	
Power Supply Ripple Voltage		VRP	-	-	600	mV	
Power Supply Current		IDD	-	0.76	2.2	A	Note 1
Power Consumption		PDD	-	9.1	26.4	Watt	
Rush current		IRUSH	-	-	10	A	Note 2
V by One Interface	Differential Input High Threshold Voltage	VLVTH	-	-	+50	mV	
	Differential Input Low Threshold Voltage	VLVTL	-50	-	-	mV	
	Common Input Voltage	VLVC	-	-	-	V	
	Terminating Resistor	Rt	90	100	110	ohm	
CEDS Interface	Transmission Line Impedance	Z0	-	50	-	ohm	
	Input termination Resistance	Ri	90	100	110	ohm	
CMOS Interface	Input High Threshold Voltage	VIH	2.0	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.8	V	

Note 1 : The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for VDD=12.0V.
Frame rate f_V=60Hz and Clock frequency = 74.25MHz.
Test Pattern of power supply current.

a) Typ : Mosaic 7X5 (L0/L255) b) Max : Horizontal 1 Line (L0/L255) c) Flicker Test Pattern





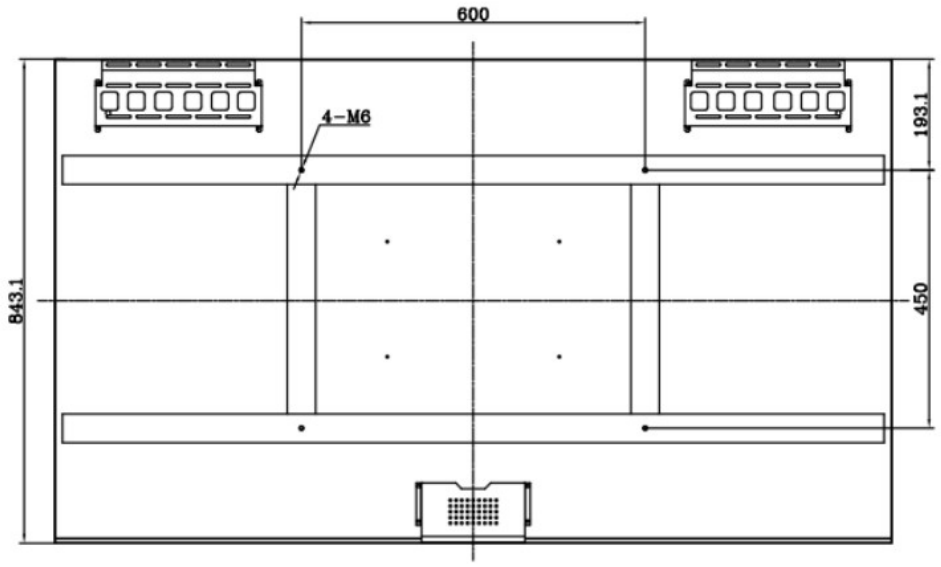


2 : The duration of rush current is about 2ms and rising time of power input is 1ms(min)

4.3.2 BACKLIGHT UNIT

parameter		Symbol	VALUES			Unit	Notes
			MIN	TYP	MAX		
Power supply input voltage		VBL	23	24	25	VDC	1
Power supply input current		IBL_A		5.3		A	1500 cd/m²
Power consumption		PBL		207		W	
Power supply input current		IBL_A		6		A	2000 cd/m²
Power consumption		PBL		264		W	
Power supply input current		IBL_A		6.9		A	2500 cd/m²
Power consumption		PBL		319		W	
Power supply input current		IBL_A		7.7		A	3000 cd/m²
Power consumption		PBL		378		W	
Input signal for inverter control	on	V on	2.5		5	V	
	off	V off	0		0.5	V	
Brightness adjust		EXTVBR-B	30		100	%	Automatic sensitization control

Rear view of LCM



Note:Any one can be selected as the main control board

LED constant current board interface

Board A

P001 PH2.0-14PIN (2.0mm*14) P002 PH2.0-2PIN (2.0mm*2)

Pin NO.	symbol	P001 Description	P002 Description	note
1	VCC	Power Supply Voltage	Light sensor negative pole -	
2	VCC	Power Supply Voltage	Light sensor positive pole +	
3	VCC	Power Supply Voltage		
4	VCC	Power Supply Voltage		
5	VCC	Power Supply Voltage		
6	GND	Power ground		
7	GND	Power ground		
8	GND	Power ground		
9	GND	Power ground		
10	GND	Power ground		
11	NC	Not connect		
12	ON/OFF	Output enable signal		
13	NC	Not connect		
14	NC	Not connect		

Board B

P001 PH2.0-14PIN (2.0mm*14) P002 PH2.0-2PIN (2.0mm*2)

Pin NO.	symbol	P001 Description	P002 Description	note
1	VCC	Power Supply Voltage	NC	
2	VCC	Power Supply Voltage	NC	
3	VCC	Power Supply Voltage		
4	VCC	Power Supply Voltage		
5	VCC	Power Supply Voltage		
6	GND	Power ground		
7	GND	Power ground		
8	GND	Power ground		
9	GND	Power ground		
10	GND	Power ground		
11	NC	Not connect		
12	NC	Not connect		
13	NC	Not connect		
14	NC	Not connect		

4.4 INTERFACE SIGNAL TIMING SPECIFICATION

4.4.1 Signal Timing Parameters

Item		Symbols	Min	Typ	Max	Unit
Pixel Clock Frequency		1/Tc	69	74.25	77	MHz
Frame Rate		F	47	60(50)	62	Hz
Vertical	Total	T_V	2180	2250(2700)	2715	T_H
	Display	T_{VD}	2160			T_H
	Blank	T_{VB}	20	90(540)	555	T_H
Horizontal	Total	T_H	530	550	570	T_{CLK}
	Display	T_{HD}	480			T_{CLK}
	Blank	T_{HB}	50	70	90	T_{CLK}

Notes:

1.This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

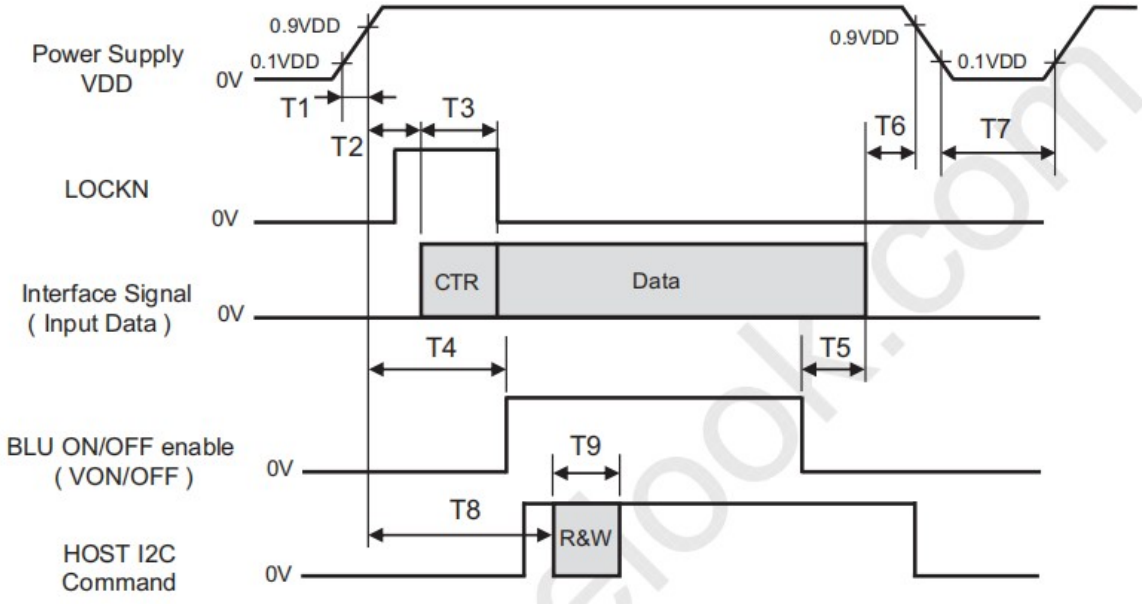
2. This product should keep clock frequency and Horizontal value fixed when adjusting frame rate.

4.4.2 V by One Input Signal Timing

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Unit Interval(VBO Operation Bit Rate)	tRBIT	3-byte	266	tTCIP/30	1667	PS
		4-byte	266	tTCIP/40	1667	PS
		5-byte	266	tTCIP/50	1667	PS
Eye Width at Package Pin	tREYE	-	-	0.5	-	UI
Eye Width Position A at Package Pin	tA	-	-	0.25	-	UI
Eye Width Position B at Package Pin	tB	-	-	0.3	-	UI
Eye Width Position Cat Package Pin	tC	-	-	0.7	-	UI
Eye Width Position D at Package Pin	tD	-	-	0.75	-	UI
Eye Width Position E at Package Pin	tE	-	-	0.7	-	UI
Eye Width Position F at Package Pin	tF	-	-	0.3	-	UI
Effective Veye level	Veye	-	-	50	-	mv
Intra – pair Skew	TTOSK_intra	-	-0.3	-	0.3	UI
Inter – pair Skew	TTOSK_inter	-	-5	-	5	UI
SSCG	-	30KHz modulation	-0.5		0.5	%

4.4.3Power Sequence

In order to get a normal display of the Open Cell, the power on/off sequence shall be as shown in below.



Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	10	ms
T2	0	-	-	ms
T3	0	-	500	ms
T4	T2+T3	-	-	-
T5	100	-	-	ms
T6	0	-	-	ms
T7	1	-	-	s
T8	T4	-	-	-
T9	Depends on I2C command			ms

Notes: 1. Even though T1 is out of SPEC, it is still ok if the inrush current of VDD is below the limit.

2. Back Light enable must after power ready for logic and interface signal are valid.

3. All input signals should set to 0 volt before VDD rising edge ready.

4. If possible, T4 should not less than hundreds of milliseconds, so do T2+T3.

5. HOST I2C should operate after BLU enable. It's used for flicker tuning. If customer does not need adjust panel flicker, ignoring T8 & T9.

6. VDD should rise and fall smoothly. If there is rebounding voltage when falling stage, it must smaller than 5 volts.

5. OPTICAL CHARACTERISTICS

5.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance≤1 lux and temperature=25±2°C) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 180cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to $\theta_{Ø=0}$ (=θ_3) as the 3 o'clock direction (the "right"), $\theta_{Ø=90}$ (= θ_{12}) as the 12 o'clock direction ("upward"), $\theta_{Ø=180}$ (= θ_9) as the 9 o'clock direction ("left") and $\theta_{Ø=270}$(= θ_6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 12.0V +/-10% at 25°C. Optimum viewing angle direction is 6 'clock.

< Optical Specifications>

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	Θ_3	CR > 10	-	89	-	Deg.	Note1
		Θ_9		-	89	-	Deg.	
	Vertical	Θ_{12}		-	89	-	Deg.	
		Θ_6		-	89	-	Deg.	
Contrast ratio		CR	Θ = 0° (Center) Normal Viewing Angle	1000	1200	-		Note2
Reproduction of color	White	W_x		-0.03	0.282	+0.03	-	Based on BOE Back-klight
		W_y			0.315		-	
	Red	R_x			0.637		-	
		R_y			0.334		-	
	Green	G_x			0.301		-	
		G_y			0.620			
	Blue	B_x			0.154		-	
		B_y			0.061		-	
Response Time	G to G	T_g		-	8	10	ms	Note4
Gamma Scale				2.0	2.2	2.4	-	
Cell Transmittance				4.59	5.10		%	Note 5

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of $\theta = 0°$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See Figure 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in Table 15 shall be calculated from the spectral data measured with all pixels first in red, green, blue. Measurements shall be made at the center of the panel. The BLU is used by BOE.
4. Response time Tg is the average time required for display transition by switching the input signal as below table and is based on Frame rate fV =60Hz to optimize.
   Each time in below table is defined as Figure 2 and shall be measured by switching the input signal for "any level of gray(bright)"and "any level of gray(dark)"

Measured Response Time		Target																
		0	15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255
Start	0																	
	15																	
	31																	
	47																	
	63																	
	79																	
	95																	
	111																	
	127																	
	143																	
	159																	
	175																	
	191																	
	207																	
	223																	
	239																	
	255																	

5. Definition of Transmittance (T%) :
   Module is with white(L255) signal input

$$\text{Transmittance} = \frac{\text{Luminance of LCD Module}}{\text{Luminance of BLU}} \times 100\ \%$$

6.RELIABILITY TEST ITEM

The Reliability test items and its conditions are shown in below.

<Reliability Test Parameters >

No	Test Items	Conditions
1	High temperature storage test	Ta = 60 ℃, 240 hrs
2	Low temperature storage test	Ta = -20 ℃, 240 hrs
3	High temperature & high humidity operation test	Ta = 50 ℃, 80%RH, 240hrs
4	High temperature operation test	Ta = 50 ℃, 240hrs
5	Low temperature operation test	Ta = 0 ℃, 240hrs
6	Thermal shock	Ta = -20 ℃ ↔ 60 ℃ (0.5 hr), 100 cycle

7. MECHANICAL OUTLINE DIMENSION