SPECIFICATION
FOR
LCM+CTP Module

MODULE No:	KD058UXFLA002-C001A
CUSTOMER:	

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

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Contents

1. Block Diagram..... 5
2. Outline dimension..... 6
3. Input terminal Pin Assignment..... 7
4. LCD Optical Characteristics..... 9
4.1 Optical specification..... 10
5. Electrical Characteristics..... 13
5.1 Absolute Maximum Rating..... 13
5.2 DC Electrical Characteristics..... 13
5.3 LED Backlight Characteristics..... 14
5.4 Operating Principle & Methods..... 16
5.4.1 SPI Interfac..... 16
5.4.2 Power ON/OFF Timing..... 18
6. Parallel RGB at DE only mode..... 22
7. CTP Specification..... 25
7.1 Electrical Characteristics..... 25
7.1.1 Absolute Maximum Rating..... 25
7.1.2 DC Electrical Characteristics (Ta=25℃)..... 25
7.1.3 AC Characteristics..... 26
7.2 I2C Timing..... 26
8. LCD Module Out-Going Quality Level..... 24
8.1 VISUAL & FUNCTION INSPECTION STANDARD..... 31
8.1.1 Inspection conditions..... 31
8.1.2 Definition..... 31
8.1.3 Sampling Plan..... 32
8.1.4 Criteria (Visual)..... 33
9. Reliability Test Result..... 37
10. Cautions and Handling Precautions..... 38
10.1 Handling and Operating the Module..... 38
10.2 Storage and Transportation..... 38
11. Packing..... 39

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorpho us silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Pan el, driver circuit,back-light unit. The resolution of a 5.8 " TFT-LCD contains 1920X1080 pixels, and can display up to 16.7M colors.

* Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	126.72(H)*71.28(V) (5.8 inch)	mm	
Driver element	TFT active matrix	-	
Display colors	262K	colors	
Number of pixels	1920(RGB)*1080	dots	
Pixel arrangement	RGB vertical stripe	-	
Pixel pitch	0.066(H)*0.066(V)	mm	
Viewing angle	ALL	o'clock	
Display mode	Transmissive/Normally Black	-	
D-IC	HX8286*3 HX8695*1		
LCM Interface	8BIT LVDS	-	
Operating temperature	-20～+70	℃	
Storage temperature	-30～+80	℃	

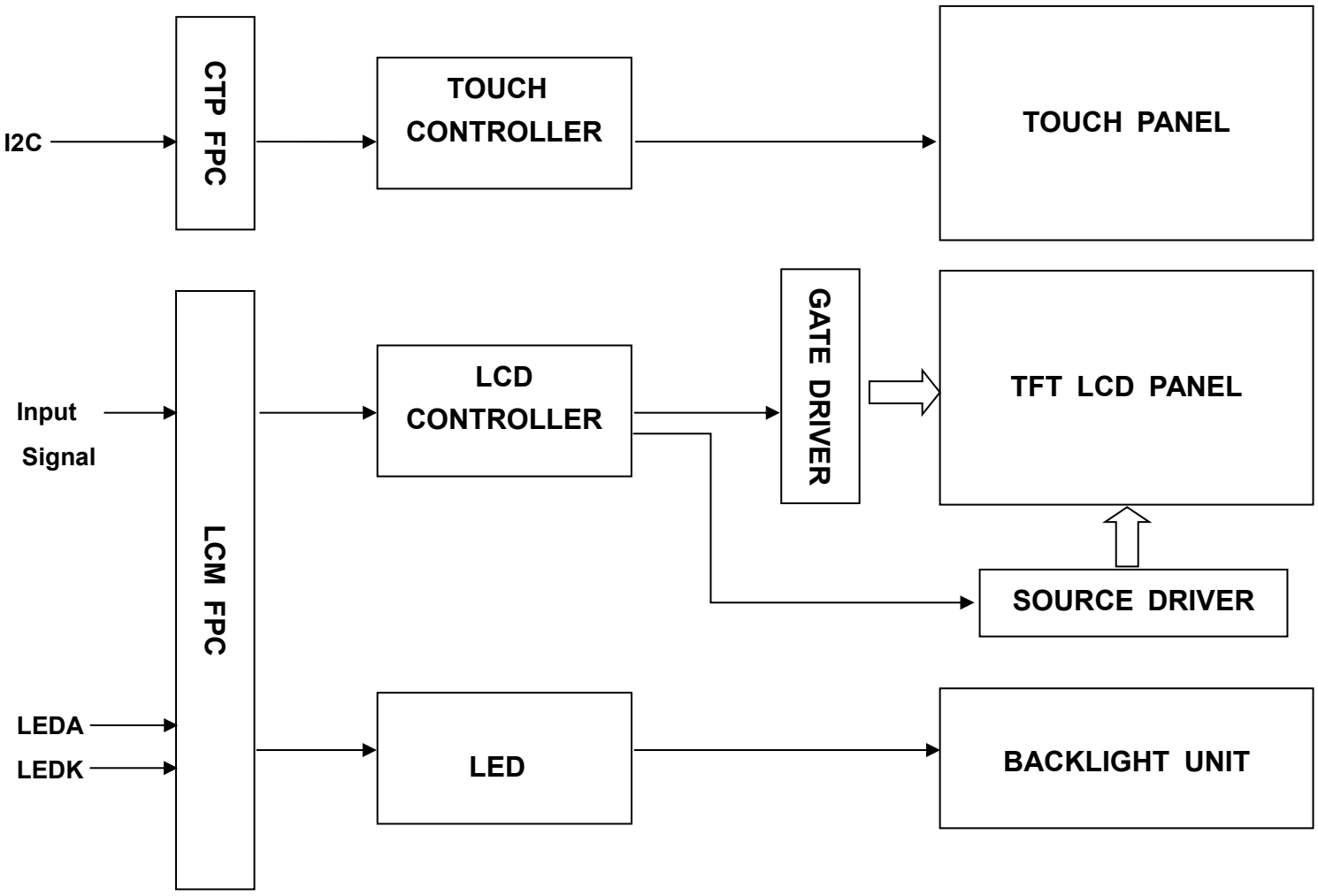
* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	144.56	-	mm	
	Vertical(V)	-	87.40	-	mm	
	Depth(D)	-	7.65	-	mm	
Weight		-	TBD	-	g	

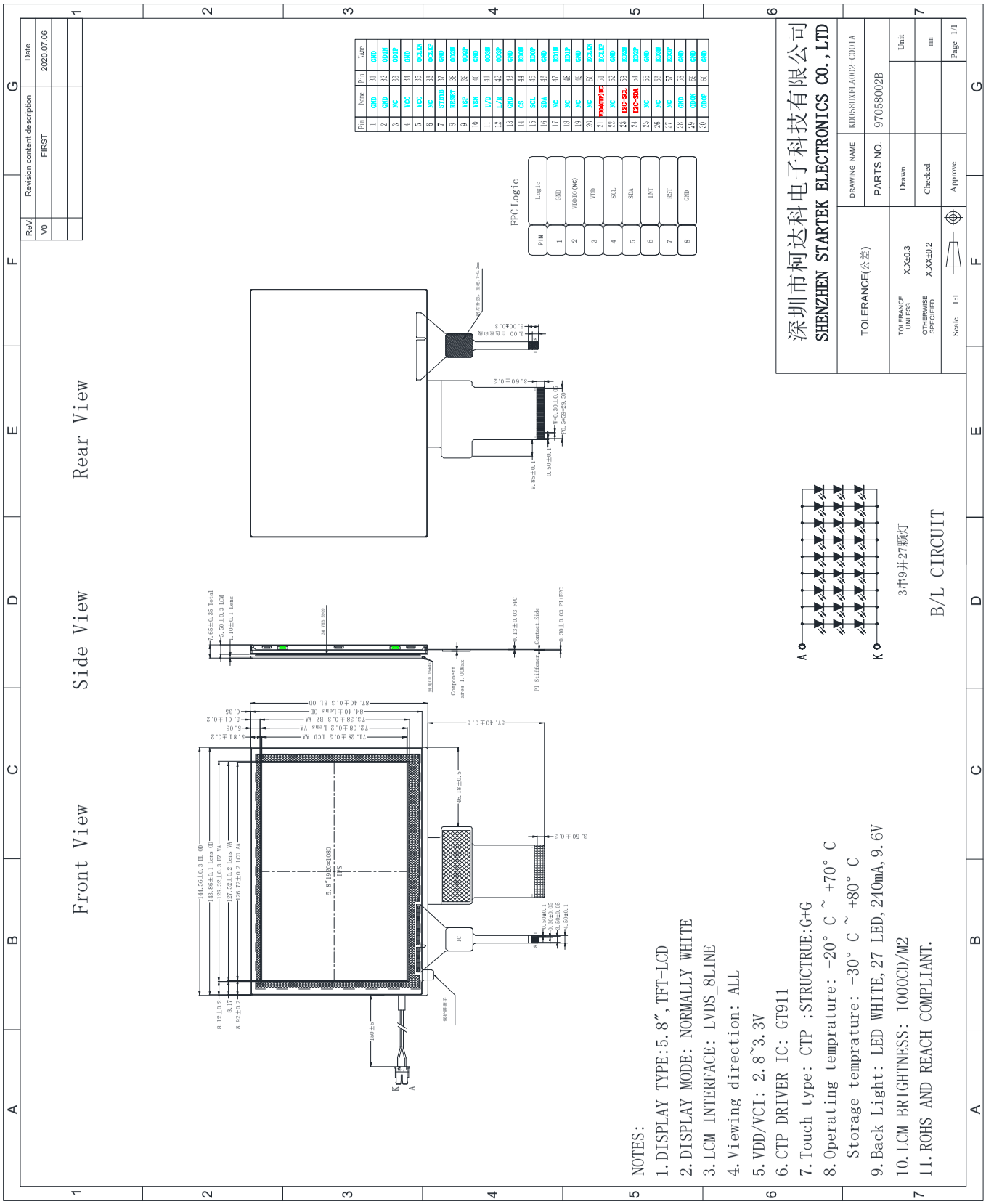
*CTP Features

General Information Items	Specification	Unit	Note
	Main Panel		
Resolution	720(H)*1280(V)	-	
Structure	G+G	-	
Controller IC	GT911	-	
Interface	I2C	-	
Slave Adress	0x5D(7bit) or 0x14(7bit)	-	Note1
Touch mode	Five points and Gestures	-	-
Logic level	3.3	V	

1. Block Diagram



2. Outline dimension



3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	GND	Ground.	P
3	NC	No connection.	
4	VCC	Supply voltage (3.3V).	P
5	VCC	Supply voltage (3.3V).	P
6	NC	No connection.	
7	STBYB	STBYB= “H”， normal operation(default)	I
8	RESET	Reset pin. The chip is in reset state when RESETB=0.	I
9	VSP	Positive input analog power for driver IC use 5~7V	P
10	VSN	Positive input analog power for driver IC use -5~-7V	P
11	U/D	Gate up or down scan control	I
12	L/R	Source right or left sequence control	I
13	GND	Ground.	P
14	SPI_CS	Chip select input pin (“Low” enable).	I
15	SPI_SCL	Serial clock	I
16	SPI_SDA	Serial DATA input signal	I
17	NC	No connection.	
18	NC	No connection.	
19	NC	No connection.	
20	NC	No connection.	
21	VDD(OTP)NC	No connection.	
22	NC	No connection.	
23	I2C-SCL	I2C clock input.	I
24	I2C-SDA	I2C data input and output	I/O
25	NC	No connection.	

26	I2C/SPI_SET	I2C/SPI_SET NC=SPI 3.3V=I2C	I
27	NC	No connection.	
28	GND	Ground.	P
29	OD0N	Mini-LVDS data input	I
30	OD0P	Mini-LVDS data input	I
31	GND	Ground.	P
32	OD1N	Mini-LVDS data input	I
33	OD1P	Mini-LVDS data input	I
34	GND	Ground.	P
35	OCLKN	Mini-LVDS Clock input	I
36	OCLKP	Mini-LVDS CLock input	I
37	GND	Ground.	P
38	OD2N	Mini-LVDS data input	I
39	OD2P	Mini-LVDS data input	I
40	GND	Ground.	P
41	OD3N	Mini-LVDS data input	I
42	OD3P	Mini-LVDS data input	I
43	GND	Ground.	P
44	ED0N	Mini-LVDS data input	I
45	EDOP	Mini-LVDS data input	I
46	GND	Ground.	P
47	ED1N	Mini-LVDS data input	I
48	ED1P	Mini-LVDS data input	I
49	GND	Ground.	P
50	ECLKN	Mini-LVDS Clock input	I
51	ECLKP	Mini-LVDS Clock input	I
52	GND	Ground.	P

53	ED2N	Mini-LVDS data input	I
54	ED2P	Mini-LVDS data input	I
55	GND	Ground.	P
56	ED3N	Mini-LVDS data input	I
57	ED3P	Mini-LVDS data input	I
58	GND	Ground.	P
59	GND	Ground.	P
60	GND	Ground.	P

CTP PIN Define

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground	P
2	NC	No Connection	
3	VDD	Supply voltage	P
4	SCL	I2C clock input	I
5	SDA	I2C data input and output	I
6	INT	External interrupt to the host	I
7	RST	External Reset, Low is active	I
8	GND	Ground	P

4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal viewing angle	--	800	--		(1)(2)
Response time	Rising	$T_{R+}T_F$		--	25	30	msec	(1)(3)
	Falling							
Color Gamut		S(%)		--	54	--	%	C-light
Color Filter Chromacicity	White	W_X		0.2893	0.2896	0.2915		(1)(4) CF glass
		W_Y		0.3342	0.3350	0.3353		
	Red	R_X		0.6003	0.6012	0.6015		
		R_Y		0.3350	0.3354	0.3356		
	Green	G_X		0.2943	0.2944	0.2954		
		G_Y		0.5468	0.5469	0.5483		
	Blue	B_X		0.1468	0.1470	0.1477		
		B_Y		0.0909	0.0925	0.0930		
Viewing angle	Hor.	ΘL	CR>10	--	85	--		(1)(4)
		ΘR		--	85	--		
	Ver.	ΘU		--	85	--		
		ΘD		--	85	--		
Option View Direction		ALL						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding : dark room

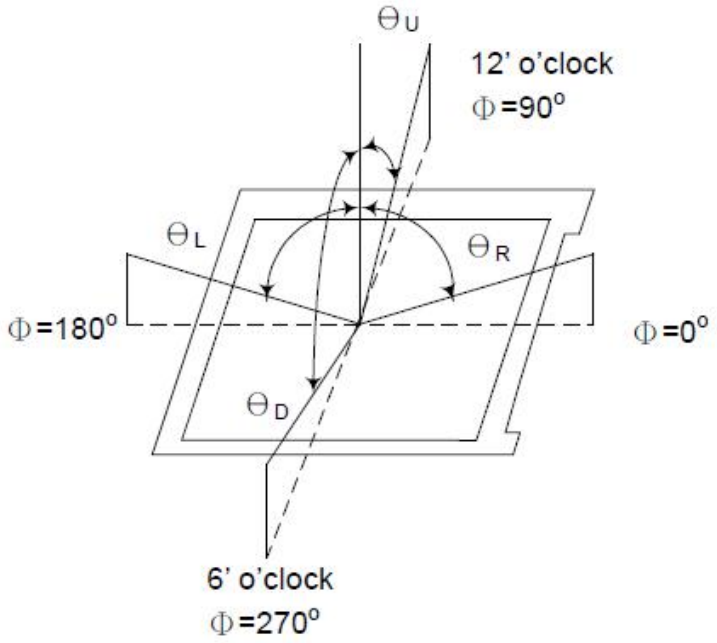
Ambient temperature : 25±2°C

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

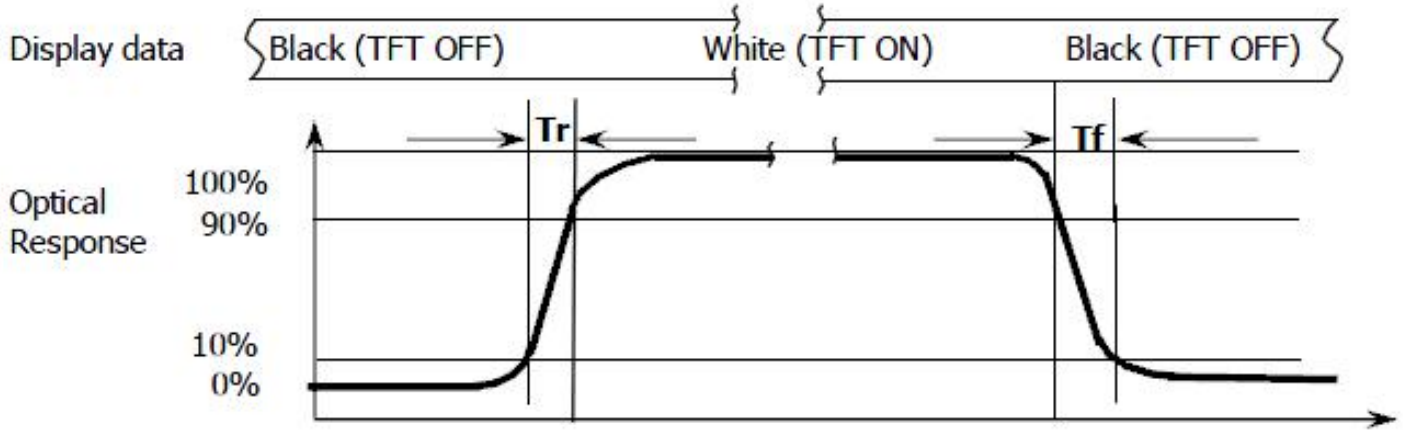
Note (1): Definition of Viewing Angle :



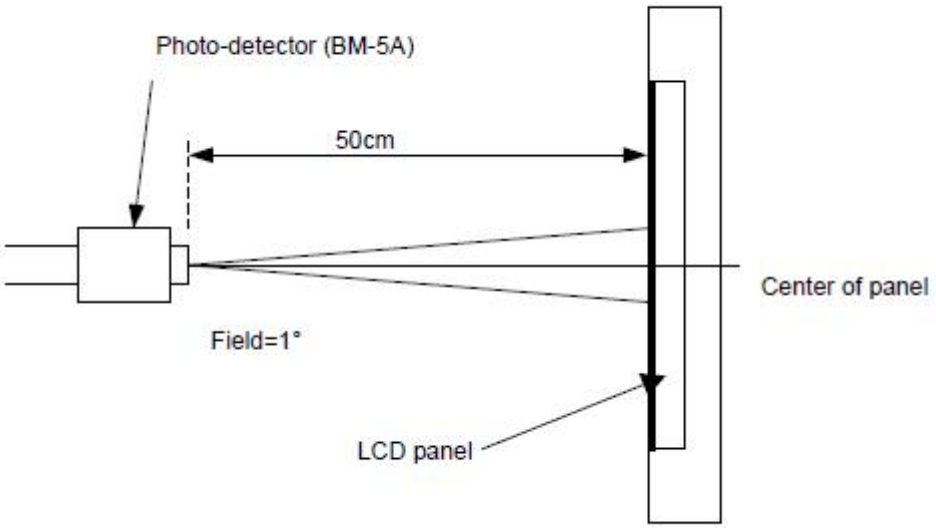
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



5. Electrical Characteristics

5.1 Absolute Maximum Rating

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. Make sure all the design characteristics are adequate before the panel is initialed. All the measurements should be operated with driver IC and FPC mounted.

Parameter	Symbol	Min	Max	Unit	Remark
LC Operating Voltage *1)	V_{op}	TBD	TBD	V	Ta= 25℃
Operating Temperature	T_{OP}	-20	+70	℃	
Storage Temperature	T_{ST}	-30	+80	℃	
Operating Ambient Humidity *2)	Hop	10	*3)	%RH	*3)
Storage Humidity	Hst	10	*3)	%RH	*3)

Note: **[VSS = GND = 0V]**

1. Liquid Crystal driving voltage: Due to the characteristics of LC Material, this voltage varies with environmental temperature
2. Temp≤60℃ 90% RH MAX
3. Non-condensation

5.2 DC Electrical Characteristics

GND=0V, VDD=3.3V, Ta = 25℃

Item		Symbol	MIN	TYP	MAX	Uni	Remar
Logic Supply Voltage		VDD	2.3	3.3	3.6	tV	k
Input Signal Voltage	High Level	VIH	0.7*VDD	-	VDD	V	
	Low Level	VIL	0	-	0.3*VDD	V	
Output Signal Voltage	High Level	VOH	VDD-0.4	-	VDD	V	
	Low Level	VOL	0	-	0.4	V	
Mini-LVDS	High Level	VIHLVDS	200	-	400	mV	
	Low Level	VILLVDS	-200	-	400	mV	
	Com Level	VCMLVDS	GND+0.8	1.2	VDD-1.5	V	
Logic Supply Voltage		AVDD	(10.7)	(10.9)	(11.1)	V	
		VGH	(19.0)	(20.0)	(21.0)	V	
		VGL	(-6.5)	(-7.0)	(-7.5)	V	
		Vcom	(3.4)	(3.92)	(4.8)	V	
Power Consumption		Black Mode	-	TBD	-	m W	

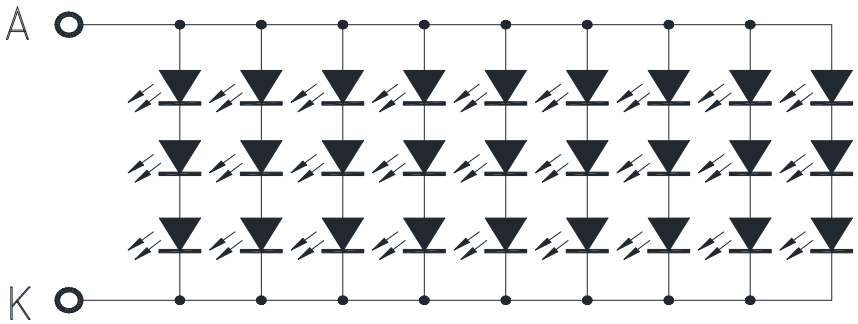
5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 27 chips LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	--	240	--	mA	
Forward Voltage	V_F	--	9.6	--	V	
LCM Luminance	LV	--	1000	--	cd/m2	Note3
LED life time	Hr	--	50000	--	Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

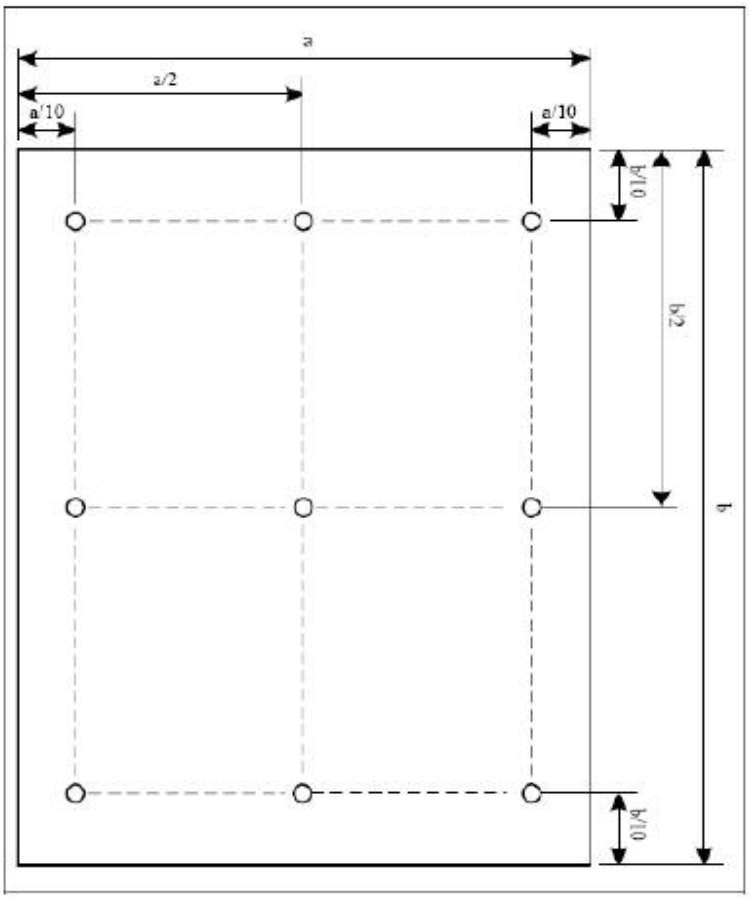
Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=240mA. The LED lifetime could be decreased if operating IL is larger than 240mA. The constant current driving method is suggested.



3串9并27颗灯

B/L CIRCUIT

Note (3) Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

5.4 Operating Principle & Methods

5.4.1 SPI Interface

supports 3/4-wire SPI **(serial peripheral interface)** to set internal registers. Setting one command needs 16 SCL clocks.

A. The first bit R/W selects read/write mode. Setting R/W to 0 selects write mode, and setting R/W to 1 selects read mode.
B. If there are two chips or three chips cascaded, the second and third bits SID [1:0] select chip being active. Note that when SIDEN=0 and R/W=1, only read from the master chip.
C. Short the SDAI and SDAO together for 3-wire SPI.

SIDEN	R/W	SID[1:0]	Function	Target
0	1	xx	Read	Master
	0	xx	Write	Master and slave
1	1	00	Read	Master
		01		Slave1
		10		Slave2
		11		Slave3
	0	00	Write	Master
		01		Slave1
		10		Slave2
		11		Slave3

Table 8.3: Serial Interface timing parameter

D. A [4:0] specify the address of the register to be read or written.
E. D [7:0] is the 8-bit data of each register.

The address and data are transferred from the MSB to LSB edge sequentially at SCL rising edge.

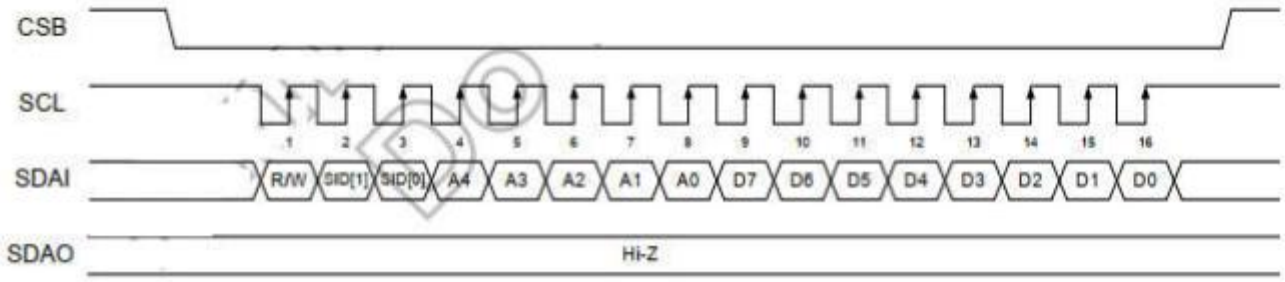


Figure 8.8: SPI format

I2C Interface

supports 2-wire serial interface (**I2C**) to set internal registers.
is a slave and the slave address is fixed 1010010.

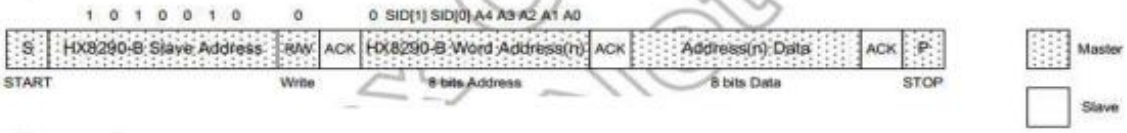
A. If there are two chips ,three chips or four chips cascaded, the second and third bits SID[1:0] select chip being active. Note that when SIDEN=0 and R/W=1, only read from the master chip.

SIDEN	R/W	SID[1:0]	Function	Target
0	1	xx	Read	Master
	0	xx	Write	Master and slave
1	1	00	Read	Master
		01		Slave1
		10		Slave2
		11		Slave3
	0	00	Write	Master
		01		Slave1
		10		Slave2
		11		Slave3

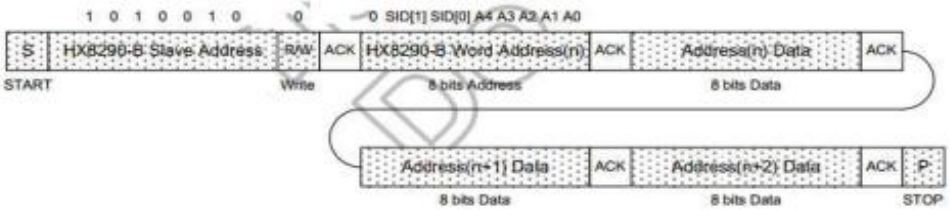
Table 8.4: Serial Interface timing parameter

B. If there are two chips ,three chips or four chips cascaded, when Master chip and slave chips received the slave address from Host, the ACK will response from Master Chip (**SID [1:0]=00**) only.

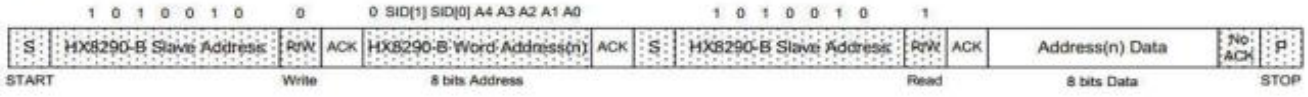
Byte write



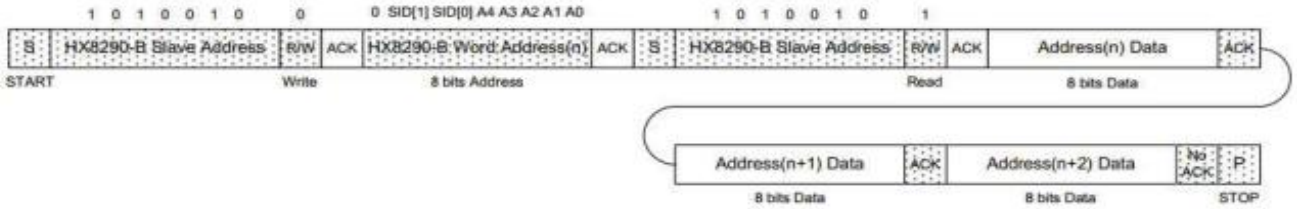
Burst write



Byte read



Burst read



5.4.2 Power ON/OFF Timing

If VSP=VSDP and VSN=VSDN by external power supply, VGH and VGL generated by internal charge pump circuits:

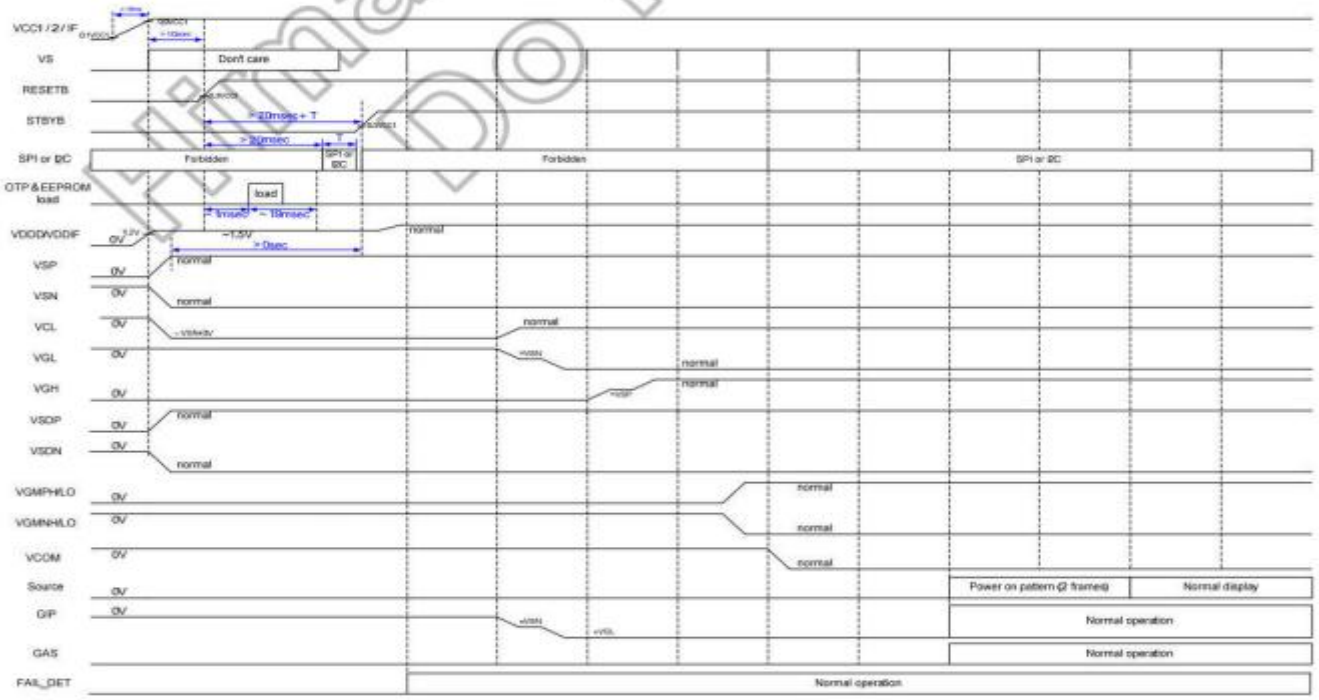


Figure Power-on sequence with external power supply

If VSP=VSDP and VSN=VSDN by external power supply, VGH and VGL generated by internal charge pump circuits:

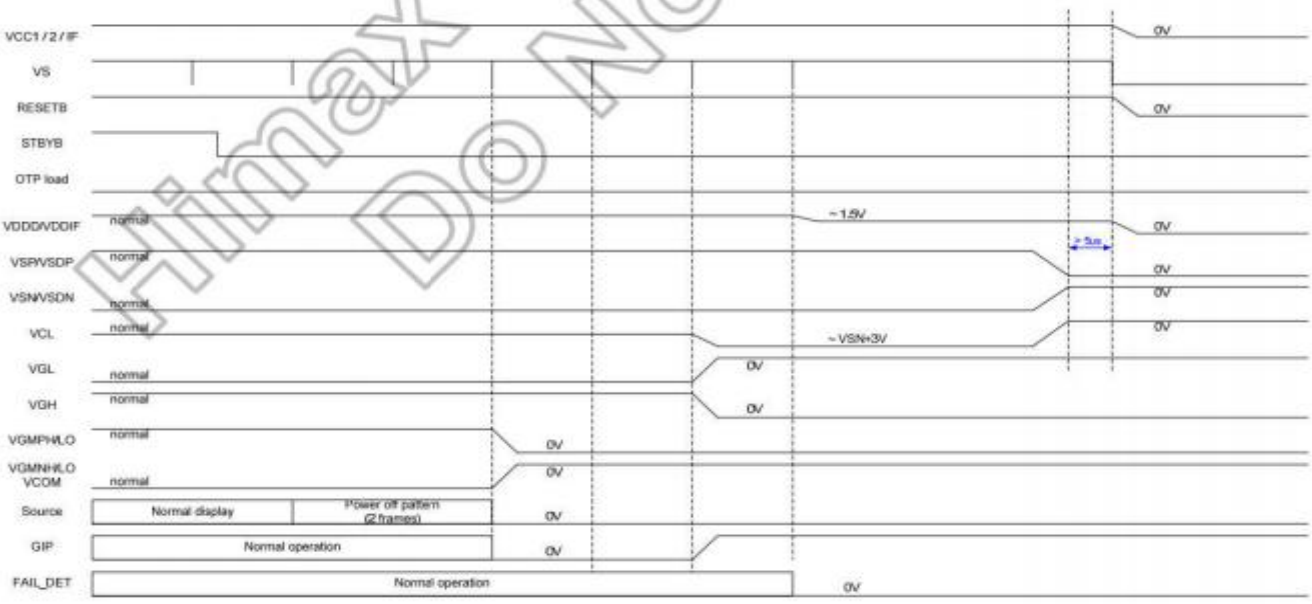


Figure Power-off sequence with external power supply

Timing

Parallel RGB at Sync mode

*Horizontal

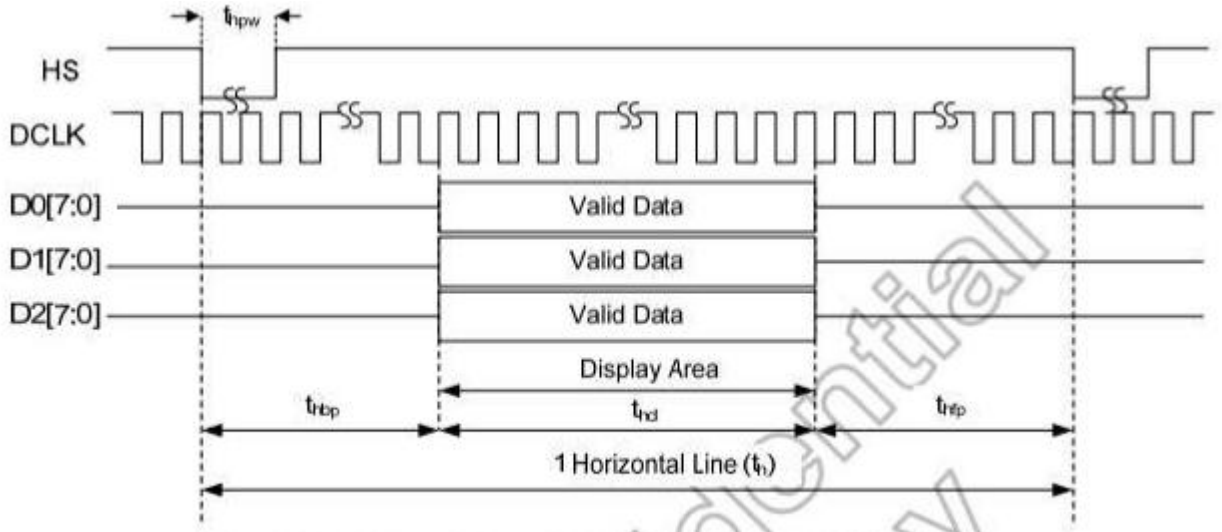


Figure 8.4: Horizontal input timing at Sync mode (CLOCKP=1)

*Vertical

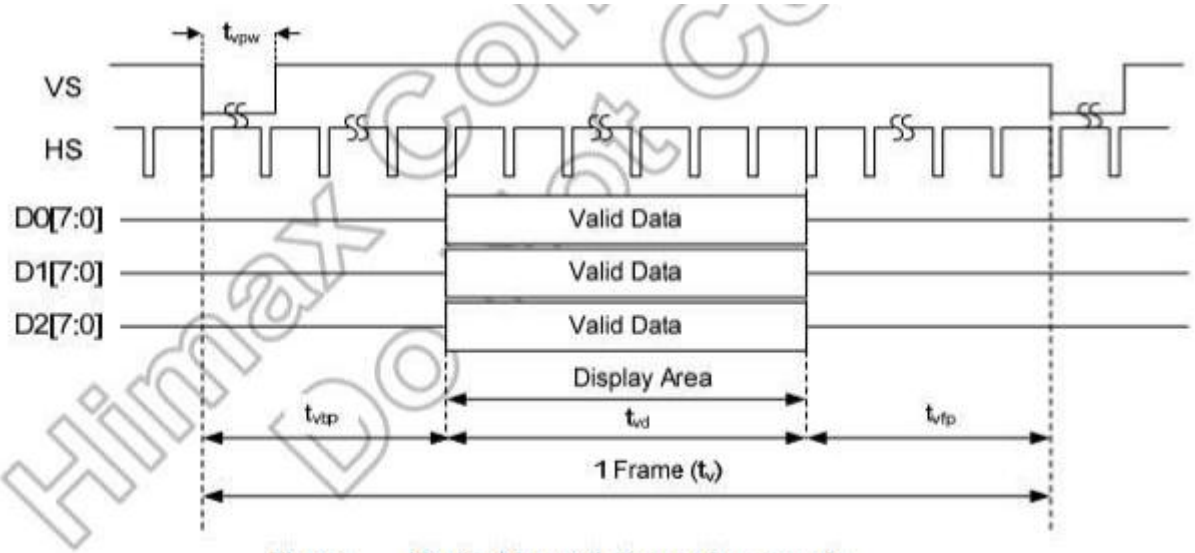


Figure Vertical input timing at Sync mode

Parameter	Symbol	Panel Resolution									Unit
		2560xRGBx720 (Two Port)			2880xRGBx1080 (Two Port)			2048xRGBx1200 (Two Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLK frequency	F_{CLK}	-	61.65	-	-	101.61	-	-	81.54	-	MHz
Horizontal valid data	t_{hd}		1280			1440			1024		CLK
Hsync pulse width	t_{hpw}	6	12	254	6	12	254	6	12	254	CLK
Hsync back porch	t_{hbp}	7	16	255	7	16	255	7	16	255	CLK
Hsync front porch	t_{hfp}	46	56	-	46	56	-	46	56	-	CLK
1 horizontal line	t_h	1333	1352	1920	1493	1512	2160	1077	1096	1536	CLK
Vertical valid data	t_{vd}		720			1080			1200		H
Vsync pulse width	t_{vpw}	1	3	254	1	3	254	1	3	254	H
Vsync back porch	t_{vbp}	2	24	255	2	24	255	2	24	255	H
Vsync front porch	t_{vfp}	6	16	-	6	16	-	6	16	-	H
1 vertical field	t_v	728	760	1080	1088	1120	1620	1208	1240	1800	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1920xRGBx720 (Two Port)			1920xRGBx400 (One Port)			1624xRGBx1000 (Two Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLK frequency	F_{CLK}	-	47.06	-	-	52.59	-	-	55.16	-	MHz
Horizontal valid data	t_{hd}		960			1920			812		CLK
Hsync pulse Width	t_{hpw}	6	12	254	6	12	254	6	12	254	CLK
Hsync back porch	t_{hbp}	7	16	255	7	16	255	7	16	255	CLK
Hsync front porch	t_{hfp}	46	56	-	46	56	-	46	56	-	CLK
1 horizontal line	t_h	1013	1032	1440	1973	1992	2880	865	884	1218	CLK
Vertical valid data	t_{vd}		720			400			1000		H
Vsync pulse width	t_{vpw}	1	3	254	1	3	254	1	3	254	H
Vsync back porch	t_{vbp}	2	24	255	2	24	255	2	24	255	H
Vsync front porch	t_{vfp}	6	16	-	6	16	-	6	16	-	H
1 vertical field	t_v	728	760	1080	408	440	600	1008	1040	1500	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1600xRGBx300 (One Port)			1560xRGBx700 (One Port)			1540xRGBx720 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLK frequency	F_{CLK}	-	34.11	-	-	72.46	-	-	73.51	-	MHz
Horizontal valid data	t_{hd}		1600			1560			1540		CLK
Hsync pulse Width	t_{hpw}	6	12	254	6	12	254	6	12	254	CLK
Hsync back porch	t_{hbp}	7	16	255	7	16	255	7	16	255	CLK
Hsync front porch	t_{hfp}	46	56	-	46	56	-	46	56	-	CLK
1 horizontal line	t_h	1653	1672	2400	1613	1632	2340	1593	1612	2310	CLK
Vertical valid data	t_{vd}		300			700			720		H
Vsync pulse width	t_{vpw}	1	3	254	1	3	254	1	3	254	H
Vsync back porch	t_{vbp}	2	24	255	2	24	255	2	24	255	H
Vsync front porch	t_{vfp}	6	16	-	6	16	-	6	16	-	H
1 vertical field	t_v	308	340	450	708	740	1050	728	760	1080	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1536xRGBx720 (One Port)			1440xRGBx540 (One Port)			1200xRGBx2048 (Two Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLK frequency	F_{CLK}	-	73.32	-	-	52.62	-	-	84.19	-	MHz
Horizontal valid data	t_{hd}		1536			1440			600		CLK
Hsync pulse Width	t_{hpw}	6	12	254	6	12	254	6	12	254	CLK
Hsync back porch	t_{hbp}	7	16	255	7	16	255	7	16	255	CLK
Hsync front porch	t_{hfp}	46	56	-	46	56	-	46	56	-	CLK
1 horizontal line	t_h	1589	1608	2304	1493	1512	2160	653	672	900	CLK
Vertical valid data	t_{vd}		720			540			2048		H
Vsync pulse width	t_{vpw}	1	3	254	1	3	254	1	3	254	H
Vsync back porch	t_{vbp}	2	24	255	2	24	255	2	24	255	H
Vsync front porch	t_{vfp}	6	16	-	6	16	-	6	16	-	H
1 vertical field	t_v	728	760	1080	548	580	810	2056	2088	3072	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1280xRGBx720 (One Port)			1080xRGBx1920 (Two Port)			960xRGBx2560 (Two Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLK frequency	F_{CLK}	-	61.65	-		71.97	-	-	86.11	-	MHz
Horizontal valid data	t_{hd}		1280			540			480		CLK
Hsync pulse Width	t_{hpw}	6	12	254	6	12	254	6	12	254	CLK
Hsync back porch	t_{hbp}	7	16	255	7	16	255	7	16	255	CLK
Hsync front porch	t_{hfp}	46	56	-	46	56	-	46	56	-	CLK
1 horizontal line	t_h	1333	1352	1920	593	612	810	533	552	720	CLK
Vertical valid data	t_{vd}		720			1920			2560		
Vsync pulse width	t_{vpw}	1	3	254	1	3	254	1	3	254	H
Vsync back porch	t_{vbp}	2	24	255	2	24	255	2	24	255	H
Vsync front porch	t_{vfp}	6	16	-	6	16	-	6	16	-	H
1 vertical field	t_v	728	760	1080	1928	1960	2880	2568	2600	3840	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution			Unit
		720xRGBx1920 (Two Port)			
		Min.	Typ.	Max.	
CLK frequency	F_{CLK}	-	50.80	-	MHz
Horizontal valid data	t_{hd}		360		CLK
Hsync pulse Width	t_{hpw}	6	12	254	CLK
Hsync back porch	t_{hbp}	7	16	255	CLK
Hsync front porch	t_{hfp}	46	56		CLK
1 horizontal line	t_h	413	432	540	CLK
Vertical valid data	t_{vd}		1920		H
Vsync pulse width	t_{vpw}	1	3	254	H
Vsync back porch	t_{vbp}	2	24	255	H
Vsync front porch	t_{vfp}	6	16		H
1 vertical field	t_v	1928	1960	2880	H
Frame rate	FR	-	60	-	Hz

Note: (1) FR **(Frame rate)**=F_{CLK} / t_h / t_v.
(2) Horizontal back-porch could be adjusted at Sync mode by register Page00h R07h.
(3) Vertical back-porch could be adjusted at Sync mode by register Page00h R06h.
(4) $t_h=t_{hbp}+t_{hfp}+t_{hd}$ and $t_v=t_{vbp}+t_{vfp}+t_{vd}$.

Table : Input timing table at Sync mode

6. Parallel RGB at DE only mode

It just needs DE signal only,when DE only mode enable.

***Horzontal**

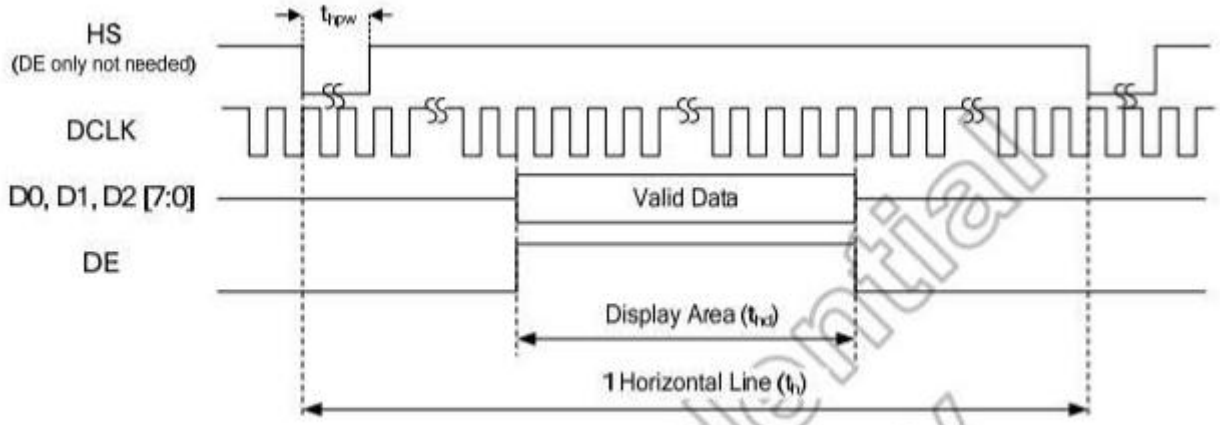


Figure 8.6: Horizontal input timing at DE only mode

***Vertical**

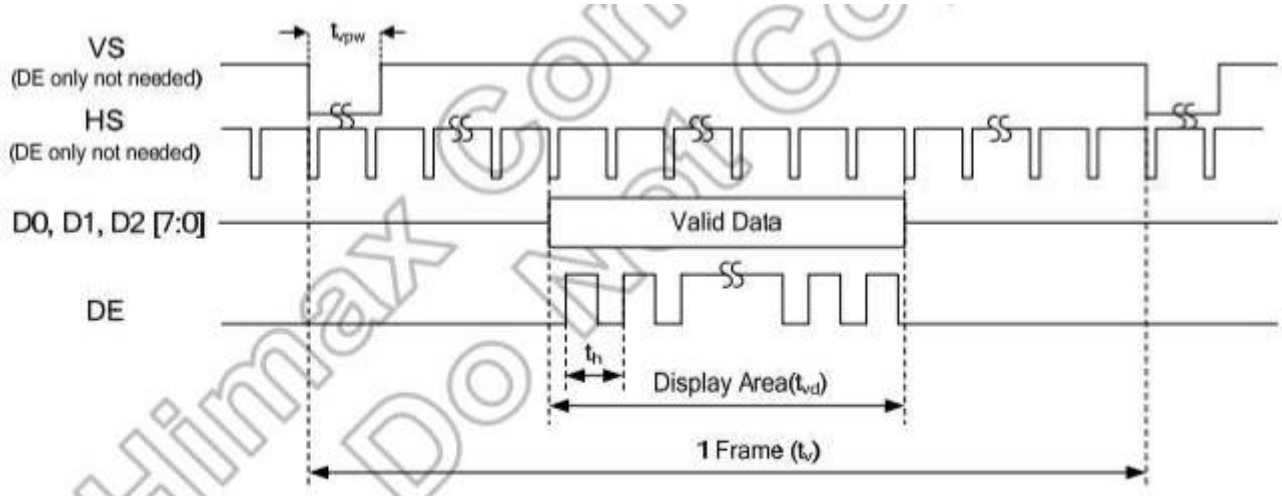


Figure Vertical input timing at DE only mode

Parameter	Symbol	Panel Resolution									Unit
		2560xRGBx960 (Two Port)			2880xRGBx1080 (Two Port)			2048xRGBx1200 (Two Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLK frequency	F_{CLK}	-	81.12	-	-	101.61	-	-	81.54	-	MHz
Horizontal valid data	t_{hd}		1280			1440			1024		CLK
1 horizontal line	t_h	1333	1352	1920	1493	1512	2160	1077	1096	1536	CLK
Vertical valid data	t_{vd}		960			1080			1200		H
1 vertical field	t_v	969	1000	1440	1088	1120	1620	1208	1240	1800	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1920xRGBx720 (Two Port)			1920xRGBx400 (One Port)			1624xRGBx1000 (Two Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLK frequency	F_{CLK}	-	47.06	-	-	52.59	-	-	55.16	-	MHz
Horizontal valid data	t_{hd}		960			1920			812		CLK
1 horizontal line	t_h	1013	1032	1440	1973	1992	2880	865	884	1218	CLK
Vertical valid data	t_{vd}		720			400			1000		H
1 vertical field	t_v	728	760	1080	408	440	600	1008	1040	1500	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1600xRGBx300 (One Port)			1560xRGBx700 (One Port)			1540xRGBx720 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLK frequency	F_{CLK}	-	34.11	-	-	72.46	-	-	73.51	-	MHz
Horizontal valid data	t_{hd}		1600			1560			1540		CLK
1 horizontal line	t_h	1653	1672	2400	1613	1632	2340	1593	1612	2310	CLK
Vertical valid data	t_{vd}		300			700			720		H
1 vertical field	t_v	308	340	450	708	740	1050	728	760	1080	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1536xRGBx720 (One Port)			1440xRGBx540 (One Port)			1200xRGBx2048 (Two Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLK frequency	F_{CLK}	-	73.32	-	-	52.62	-	-	84.19	-	MHz
Horizontal valid data	t_{hd}		1536			1440			600		CLK
1 horizontal line	t_h	1589	1608	2304	1493	1512	2160	653	672	900	CLK
Vertical valid data	t_{vd}		720			540			2048		H
1 vertical field	t_v	728	760	1080	548	580	810	2056	2088	3072	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1280xRGBx720 (One Port)			1080xRGBx1920 (Two Port)			960xRGBx2560 (Two Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLK frequency	F_{CLK}	-	61.65	-	-	71.97	-	-	86.11	-	MHz
Horizontal valid data	t_{hd}		1280			540			480		CLK
1 horizontal line	t_h	1333	1352	1920	593	612	810	533	552	720	CLK
Vertical valid data	t_{vd}		720			1920			2560		H
1 vertical field	t_v	728	760	1080	1928	1960	2880	2568	2600	3840	H
Frame rate	FR	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution 720xRGBx1920 (Two Port)			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CLK}	-	50.80	-	MHz
Horizontal valid data	t_{hd}		360		CLK
1 horizontal line	t_h	413	432	540	CLK
Vertical valid data	t_{vd}		1920		H
1 vertical field	t_v	1928	1960	2880	H
Frame rate	FR	-	60	-	Hz

Note: (1) FR **(Frame rate)**=F_{CLK} / t_h / t_v

(2) Horizontal back-porch could be adjusted at Sync mode by register Page00h R07h.

(3) Vertical back-porch could be adjusted at Sync mode by register Page00h R06h.

(4) $t_h=t_{hbp}+t_{hfp}+t_{hd}$ and $t_v=t_{vbp}+t_{vfp}+t_{vd}$

Table : Input timing table at DE only mode

7. CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	2.66	3.47	V	
Operating temperature	T_{OP}	-20	+70	℃	
Storage temperature	T_{ST}	-30	+80	℃	

7.1.2 DC Electrical Characteristics (Ta=25℃)

(Ambient temperature:25℃, VDD=2.8V, VDDIO=1.8V or VDDIO=VDD)

Item	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage/VDD	2.66	3.3	3.47	V	
Normal mode operating current	--	8	14.5	mA	
Green mode operating current	--	3.3	--	mA	
Sleep mode operating current	70	--	120	uA	
Doze mode operating current	--	0.78	--	mA	
Digital Input low voltage/VIL	-0.3	--	0.25*VDD	V	
Digital Input high voltage/VIH	0.75*VDD	--	VDD+0.3	V	
Digital Output low voltage/VOL	--	--	0.15*VDD	V	
Digital Output high voltage/VOH	0.85*VDD	--	--	V	

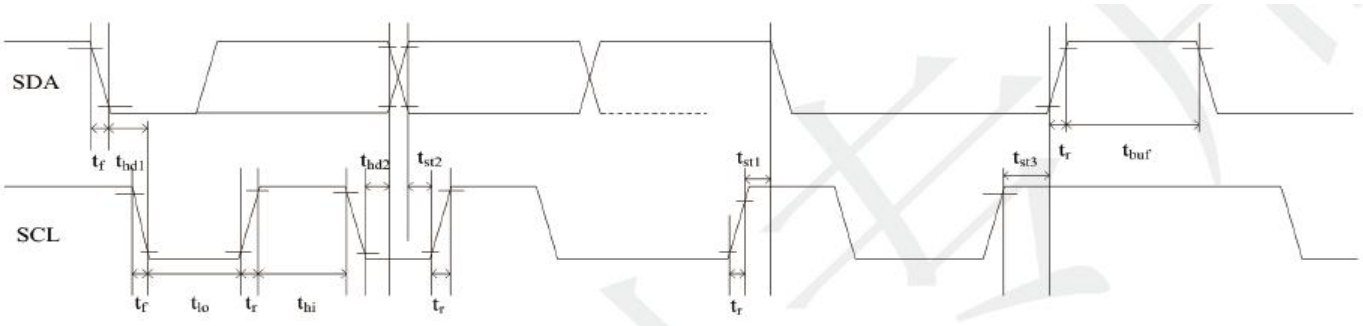
7.1.3 AC Characteristics

(Ambient temperature:25℃, VDD=2.8V, VDDIO=1.8V)

Parameter	Min	Typ	Max	Unit	Note
OSC oscillation frequency	59	60	61	MHZ	
I/O output rise time,low to high	-	14	-	ns	
I/O output rfall time,high to low	-	14	-	ns	

7.2 I2C Timing

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

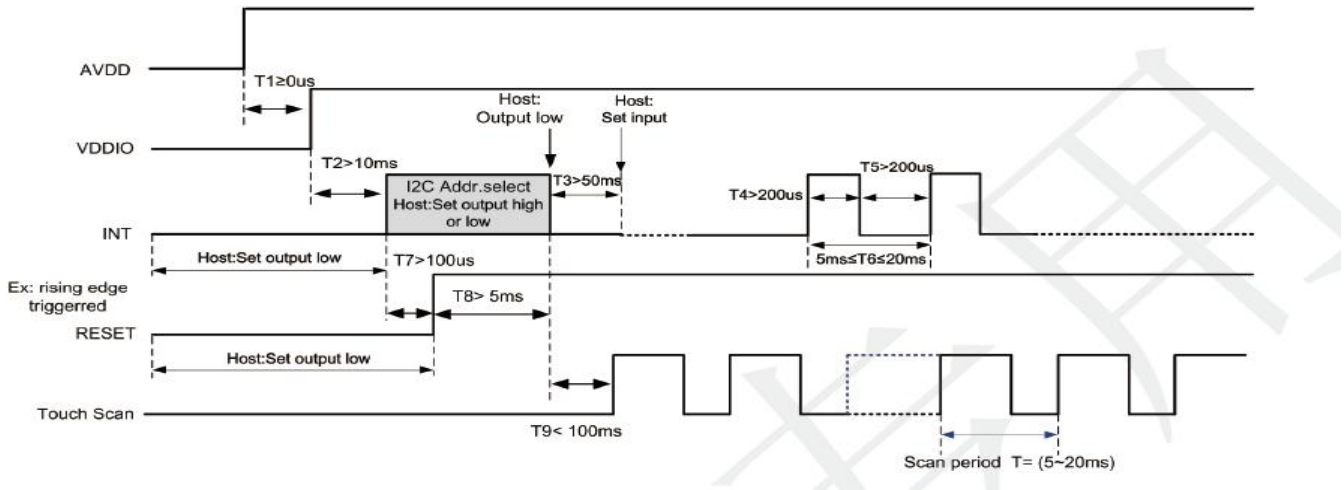
Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

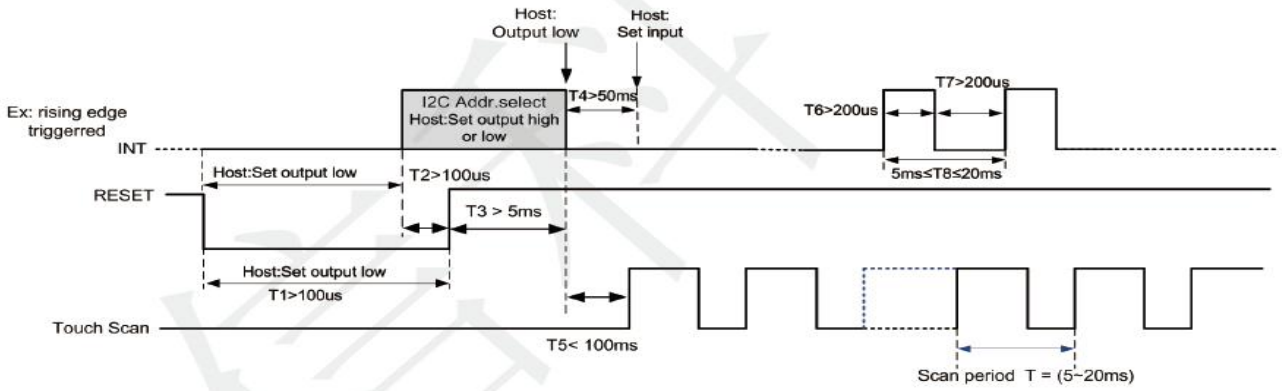
Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

GT911 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timings:

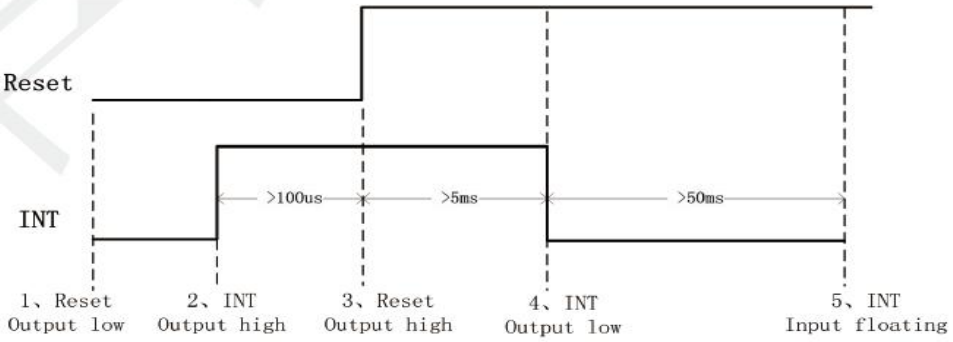
Power-on Timing:

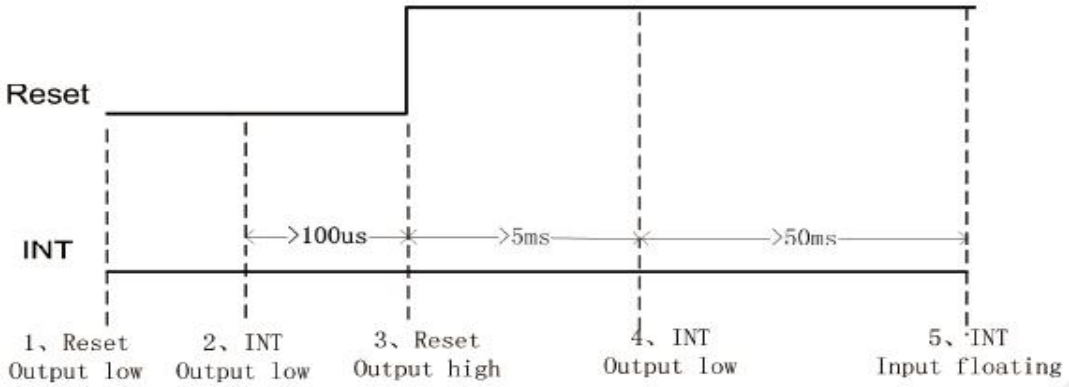


Timing for host resetting GT911:



Timing for setting slave address to 0x28/0x29:





a) Data Transmission

(For example：device address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from “high” to “low” when SCL line is “high”. Data flow or address is transmitted after the Start condition.

All slave devices connected to I²C bus should detect the 8-bit address issued after Start condition and send the correct ACK. After receiving matching address, GT911 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0XBA or 0XBB, GT911 will stay in an idle state.

For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is “high”.

When communication is completed, the host will issue the STOP condition. Stop condition implies the transition of SDA line from “low” to “high” when SCL line is “high”.

b) Writing Data to GT911

(For example：device address is 0xBA/0xBB)

Timing for Write Operation

The diagram above displays the timing sequence of the host writing data onto GT911. First, the host issues a Start condition. Then, the host sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation. Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

c) Reading Data from GT911

(For example：device address is 0xBA/0xBB)

Timing for Read Operation

The diagram above is the timing sequence of the host reading data from GT911. First, the host issues a Start condition and sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0XBB (Read Operation). After receiving ACK, the host starts to read data.

GT911 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

8. LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

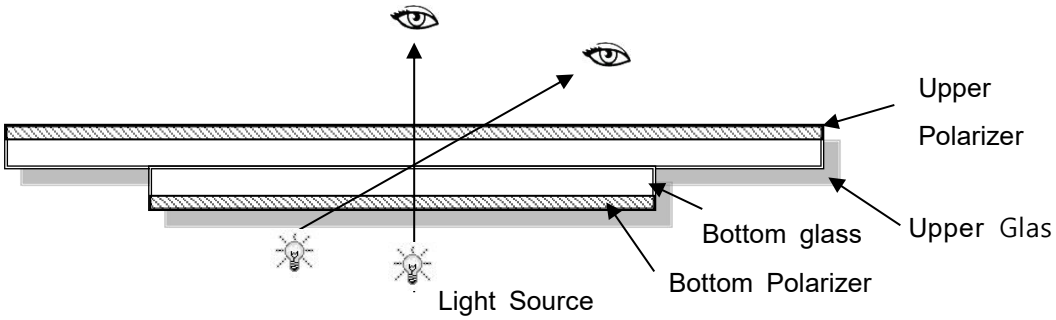
Temperature : 25±5℃

Humidity : 65%±10%RH

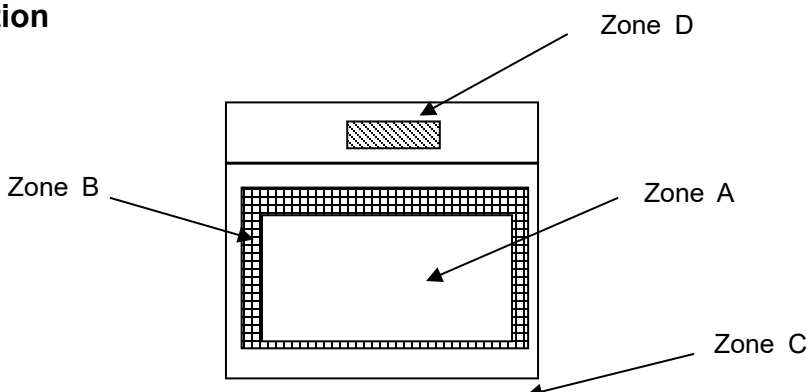
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



8.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or ap pearance after assembly by customer

8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ

AQL:

Major defect	Minor defect
0.65	1.5

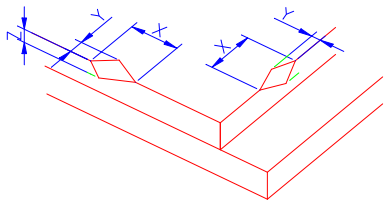
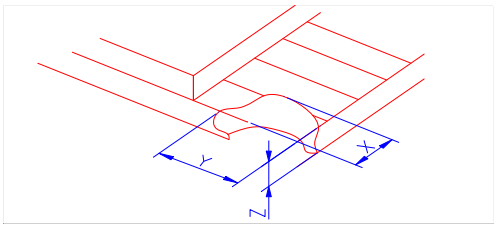
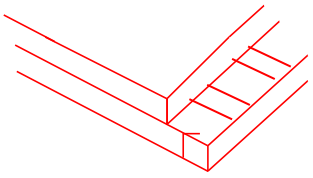
LCD: Liquid Crystal Display , LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc…	Major
2	Missing	Missing components and etc…	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed,deformation and etc	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot,Dim spot,(Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

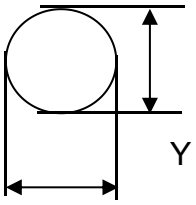
b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

8.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

2.0

Spot defect



Φ=(X+Y)/2

① light dot (black/white spot , pinhole, stain，etc.)

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧10mm)		
0.25<Φ≤0.4	2(distance≧10mm)		
Φ>0.4	0		

② Dim spot (light leakage、dent、dark spot，etc)

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧10mm)		
0.25<Φ≤0.4	2(distance≧10mm)		
Φ>0.4	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.5	2(distance≧10mm)		
Φ>0.5	0		

④Polarizer Bubble

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.4	2(distance≧10mm)		
0.4<Φ≤0.5	1		
Φ>0.5	0		

3.0 LCD Pixel defect

Pixel bad points

Item	Zone A	Acceptable Qt
Bright dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Dark dot	Random	N≤3
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm
Total bright and dark dot		N≤4

Note:

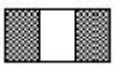
A) Bright dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

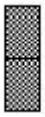
C) 2 dot adjacent = 1 pair = 2 dots

Picture:

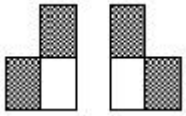
2 dot adjacent



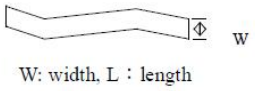
2 dot adjacent



2 dot adjacent (vertical)



2 dot adjacent (slant)

<table>
<tr>
<td>4.0</td>
<td>Line defect (LCD/RTP /Polarizer backlight black/white line, scratch, stain)
 

N：Count</td>
<td>
<table>
<tr><td rowspan="2">Width(mm)</td><td rowspan="2">Length(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.05</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L≤5.0</td><td colspan="2">N≤3</td></tr>
<tr><td>0.06<W≤0.08</td><td>L≤4.0</td><td colspan="2">N≤2</td></tr>
<tr><td>W>0.08</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td>
</tr>
<tr>
<td>5.0</td>
<td>Electronic Components SMT.</td>
<td>Not allow missing parts，solderless connection，cold solder joint，mismatch，The positive and negative polarity opposite</td>
</tr>
<tr>
<td>6.0</td>
<td>Display color& Brightness.</td>
<td>1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td>
</tr>
<tr>
<td>7.0</td>
<td>LCD Mura/Waving/ Hot spot</td>
<td>Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.</td>
</tr>
</table>

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

9. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20℃, 96HR	
High Temperature Storage	80℃, 96HR	
Low Temperature Storage	-30℃, 96HR	
High Temperature & High Humidity Operating	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-40℃,30 min ↔ 85℃,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX)	

Remark:

1.The test samples should be applied to only one test item.

2.Sample size for each test item is 5~10pcs.

3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.

4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

11. Packing

----TBD------