

**SPECIFICATION  
FOR  
LCM+CTP Module  
KD050FWFPA011-C009A**

MODULE:	KD050FWFPA011-C009A
CUSTOMER:	

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1.1	Add LCD Optical specification	2017.05.09
1.2	Update all	2018.02.28

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ISO 9001:2008

SPTS16949.2009



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### \* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 5.0" TFT-LCD contains 480x854 pixels, and can display up to 65K/262K/16.7M colors.

### \* Features

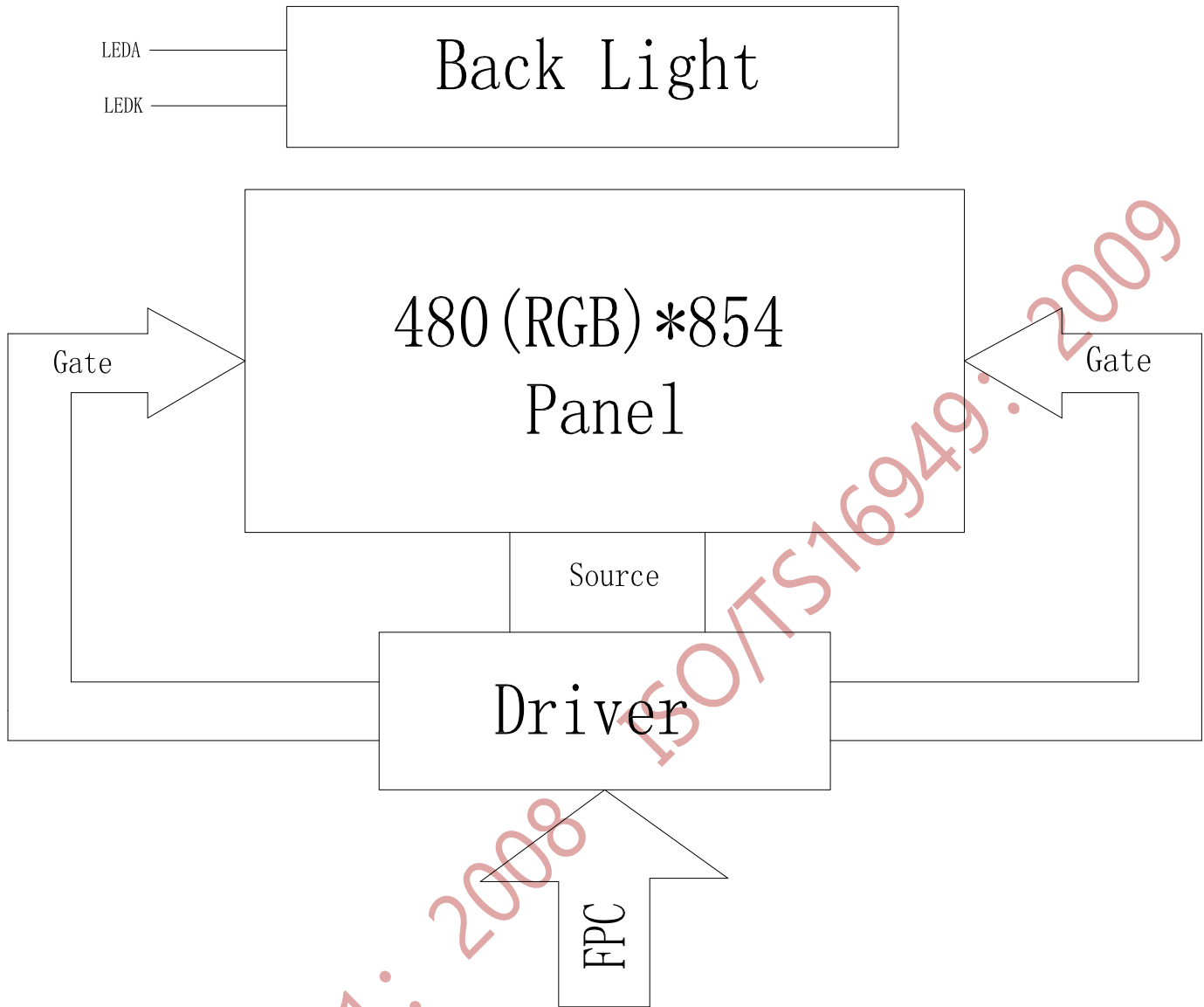
- Low Input Voltage: 3.3V(TYP)
- Display Colors of TFT LCD: 65K/262K/16.7M colors
- Interface: 3-SPI+16/18/24-bits RGB interface.
- CTP Interface: I2C

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	61.632(H)*109.6536(V) (5.0inch)	mm	-
CTP View area	62.16(H)*110.53(V)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K/16.7M	colors	-
Number of pixels	480(RGB)*854	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.1284(H)*0.1284(V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ILI9806E	-	-
CTP Driver IC	GT911	-	-
Display mode	Transmissive/Normally Black	-	-
Touch mode	5-point and Gestures	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

### \* Mechanical Information

Item	Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	67.56		mm	-
	Vertical(V)	122.35		mm	-
	Depth(D)	4.03		mm	-
Weight		--		g	-

### 1. Block Diagram



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	常备库存 Standing Stock	长期供货 Long Time supply	支持少量 NO MOQ	品种齐全 In Full Range



### 3. Input terminal Pin Assignment

#### 3.1 TFT

NO.	SYMBOL	DISCRIPTION	I/O
1	XR(NC)	Touch panel Right Glass Terminal	A/D
2	YD(NC)	Touch panel Bottom Film Terminal	A/D
3	XL(NC)	Touch panel LIFT Glass Terminal	A/D
4	YU(NC)	Touch panel Top Film Terminal	A/D
5	GND	Ground.	P
6	GND	Ground.	P
7	VCI	Supply voltage (3.3V).	P
8	IOVCC	I/O power supply voltage.	P
9	SDO	SPI interface output pin.-The data is output on the falling edge of the SCL signal.-If not used, let this pin open.	O
10	SDI	Data lane in 1 data lane serial interface. The data is latched on the rising edge of the SCL signal.	I
11	SCL	This pin is used to select "Data or Command" in the parallel interface. When D/CX = '1', data is selected. When D/CX = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. fix this pin at IOVCC or GND when not in use.	I
12	CS	Chip select input pin ("Low" enable). fix this pin at IOVCC or GND when not in use.	I
13	RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.	I
14-37	DB23-DB0	24-bit parallel bi-directional data bus for MCU system and RGB interface mode .Fix to GND level when not in use	I/O
38	DE	Data enable signal for RGB interface peration. fix this pin at IOVCC or GND when not in use.	I
39	DOTCLK	Dot clock signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.	I
40	HSYNC	Line synchronizing signal for RGB interface operation.	I

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常备库存  
Standing Stock

长期供货  
Long Time supply

支持小量  
NO MOQ

品种齐全  
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		fix this pin at VCI or GND when not in use.	
41	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.	I
42	NC		
43	LEDK	Cathode pin of backlight.	P
44	NC		
45	LEDA	Anode pin of backlight.	P

### 3.2 CTP

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	NC		
3	VDD	Supply voltage.	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P

## 4. LCD Optical Characteristics

### 4.1 Optical specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit.	Note	
Contrast Ratio	CR	$\Theta=0$ Normal viewing angle	640	800	--		(1)(2)	
Response time	Rising		$T_R$	--	16	21	msec	(1)(3)
	Falling		$T_F$	--	19	24		
Color gamut	S(%)			--	70	--	%	C-light
Color Filter Chromacity	White		$W_X$	0.264	0.304	0.344	-	(1)(4) CF glass
			$W_Y$	0.302	0.342	0.382		
	Red		$R_X$	0.602	0.642	0.682		
			$R_Y$	0.306	0.346	0.386		
	Green		$G_X$	0.280	0.320	0.360		
			$G_Y$	0.576	0.616	0.656		
	Blue	$B_X$	0.102	0.142	0.182			
		$B_Y$	0.039	0.079	0.119			
Viewing angle	Hor.	$\Theta_L$	--	80	--	-	(1)(4) Measuring with Polarizer, Reference Only	
		$\Theta_R$	--	80	--			
	Ver.	$\Theta_U$	--	80	--			
		$\Theta_D$	--	80	--			
Option View Direction			Free					

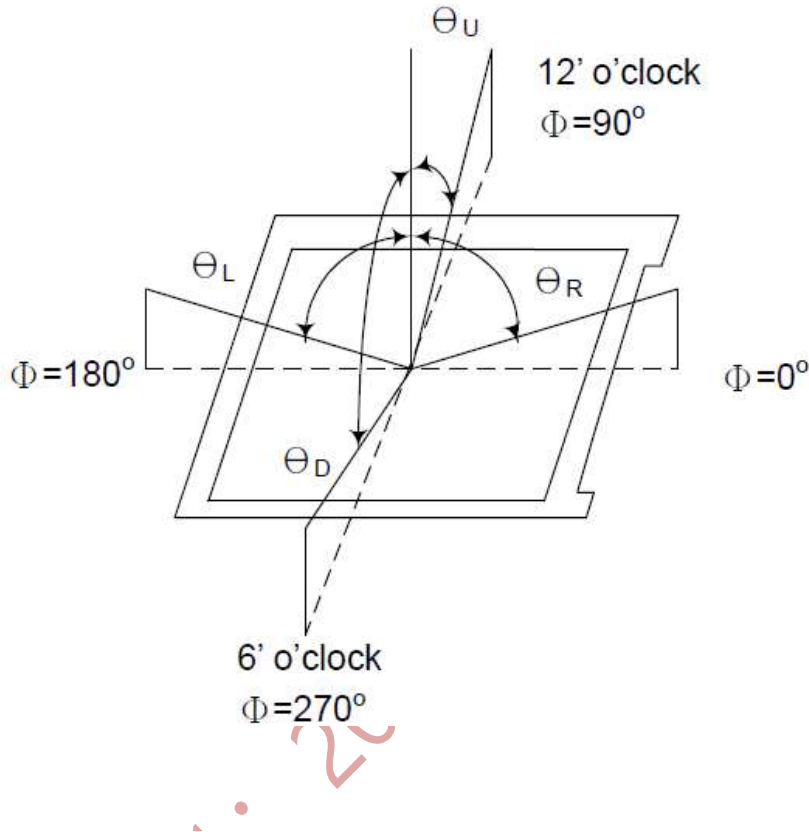
### 4.2 Measuring Condition

- Measuring surrounding: dark room
- Ambient temperature:  $25\pm 2^\circ\text{C}$
- 15min. warm-up time.

### 4.3 Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

Note (1) Definition of Viewing Angle:



Note (2) Definition of Contrast Ratio (CR) :  
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

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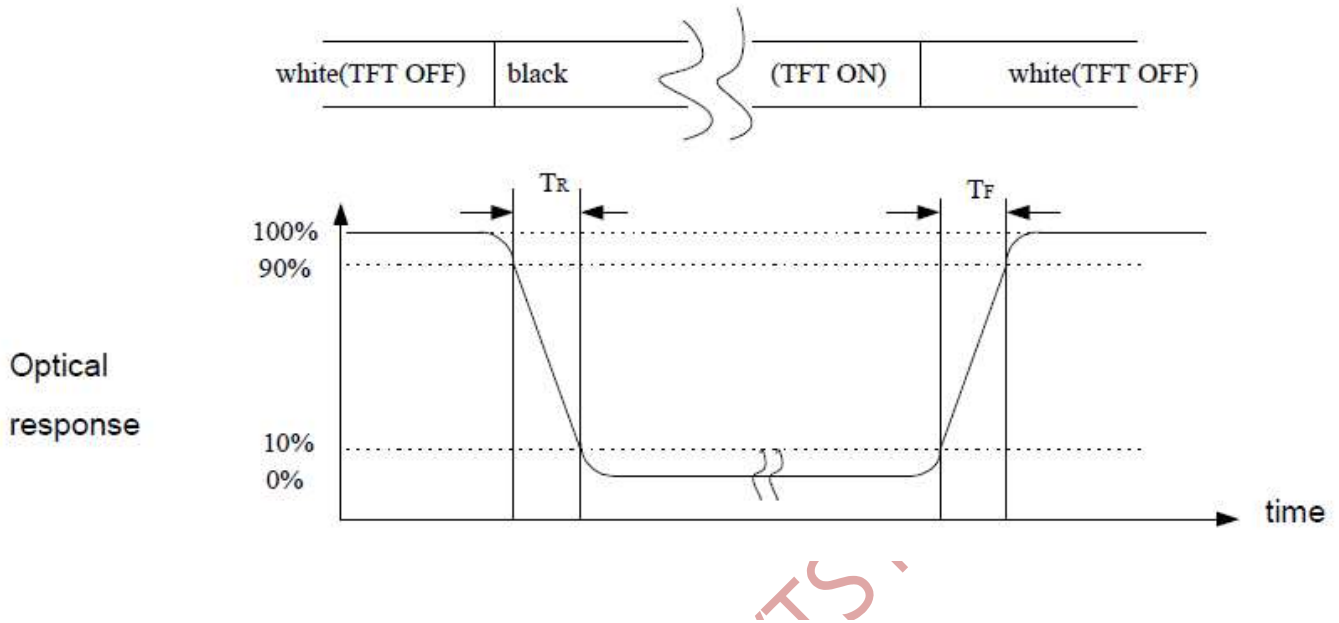
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Standing Stock

长期供货  
Long Time supply

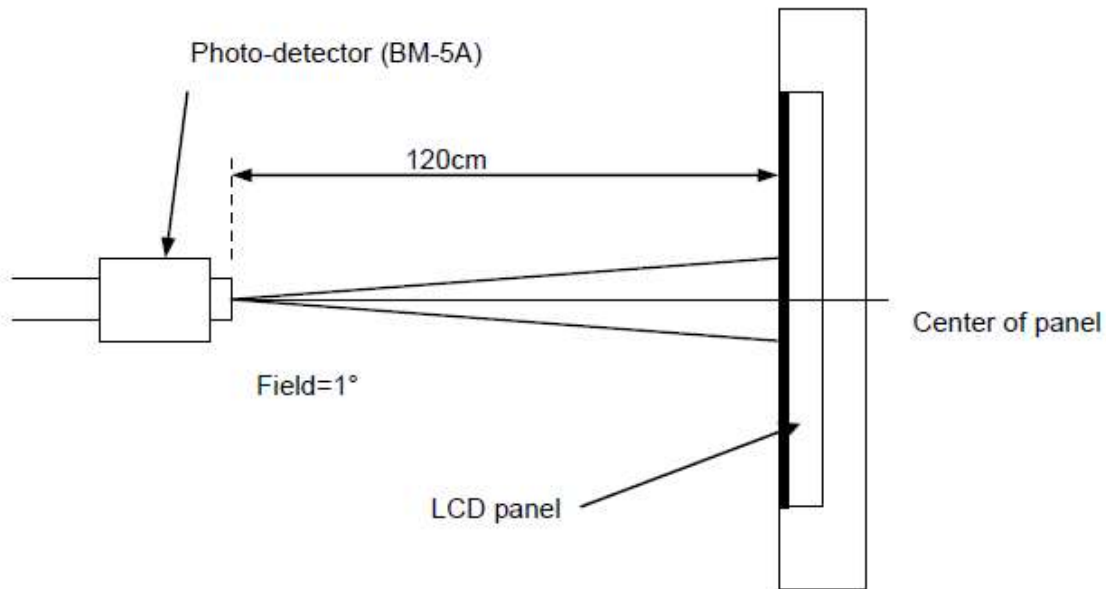
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NO MOQ

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Note (3) Definition of Response Time : Sum of  $T_R$  and  $T_F$



Note (4) Definition of optical measurement setup



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	常备库存 Standing Stock	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range

## 5. TFT Electrical Characteristics

### 5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	4.6	V
Digital interface supply Voltage	VDDIO	-0.3	4.6	V
Operating temperature	T <sub>OP</sub>	-20	+70	°C
Storage temperature	T <sub>ST</sub>	-30	+80	°C

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

### 5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.5	2.8	3.6	V	--
Digital interface supply Voltage	VDDIO	1.65	1.8	3.3	V	--
Normal mode Current consumption	IDD	--	30	--	mA	--
Level input voltage	V <sub>IH</sub>	0.7V <sub>DDIO</sub>	--	V <sub>DDIO</sub>	V	--
	V <sub>IL</sub>	-0.3	--	0.3V <sub>DDIO</sub>	V	--
Level output voltage	V <sub>OH</sub>	0.8*V <sub>DDIO</sub>	--	V <sub>DDIO</sub>	V	--
	V <sub>OL</sub>	GND	--	0.2V <sub>DDIO</sub>	V	--

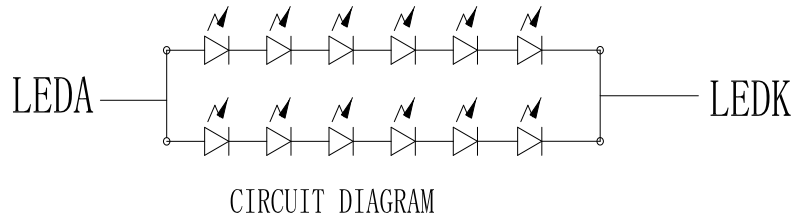
### 5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 12 chips White LED

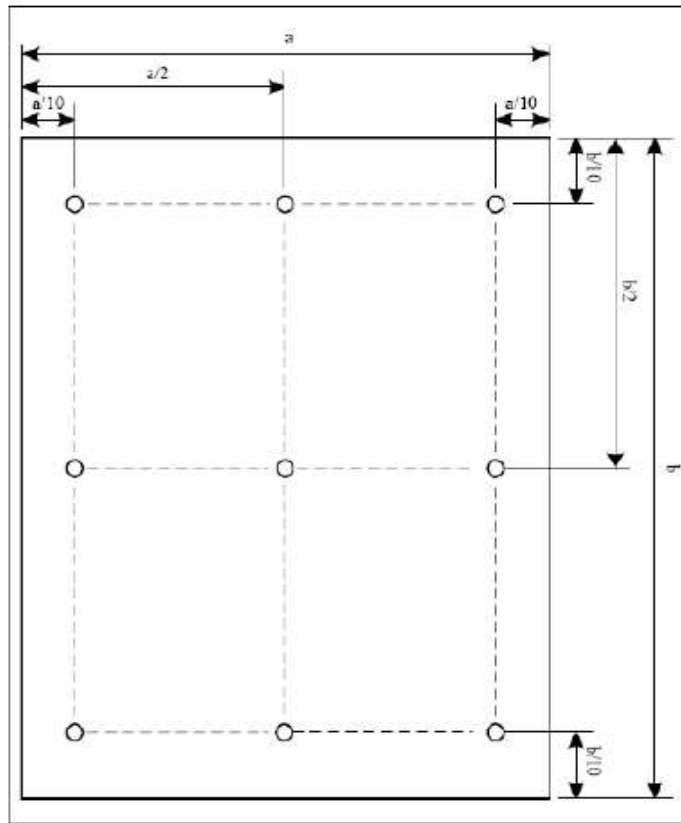
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I <sub>F</sub>	30	40	--	mA	--
Forward Voltage	V <sub>F</sub>	--	19.2	--	V	--
LCM Luminance	L <sub>v</sub>	450	500	--	cd/m <sup>2</sup>	Note3
LED life time	Hr	50000			Hour	Note1,2
Uniformity	AV <sub>g</sub>	80	--	--	%	Note3

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition:  $T_a=25\pm3\text{ }^\circ\text{C}$ , typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at  $T_a=25^\circ\text{C}$  and  $I_L=40\text{mA}$ . The LED lifetime could be decreased if operating  $I_L$  is larger than 40mA. The constant current driving method is suggested.



NOTE 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

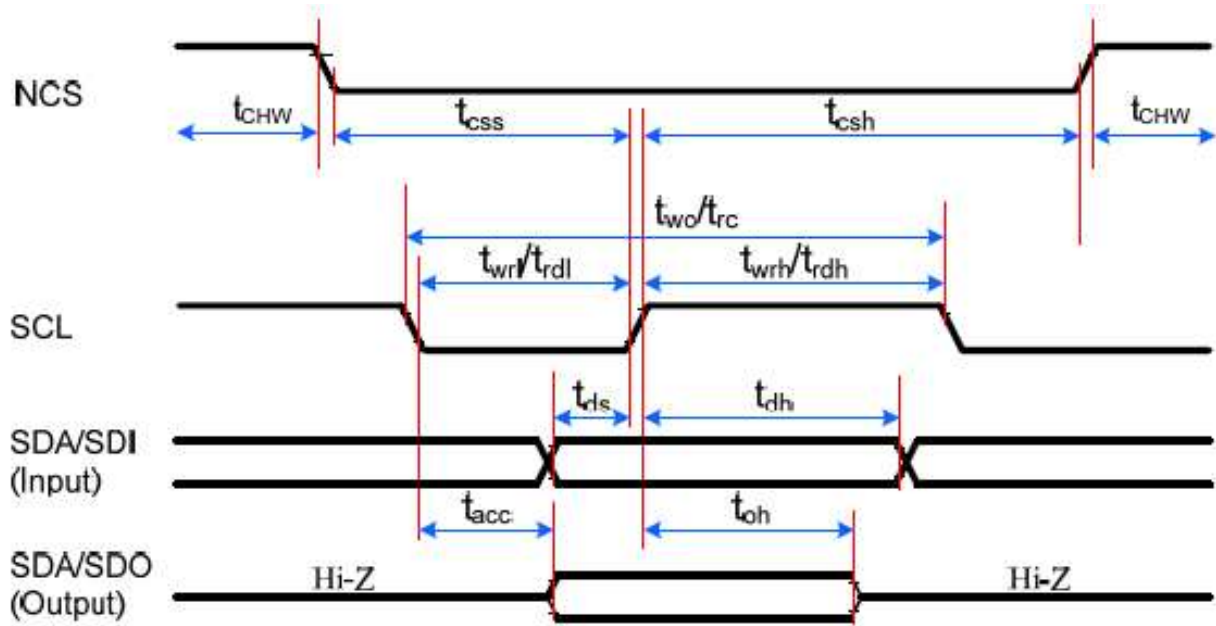
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	常备库存 Standing Stock	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range

## 6. TFT AC Characteristic

### 6.1 Display Serial Interface Timing Characteristics (3-line SPI system)

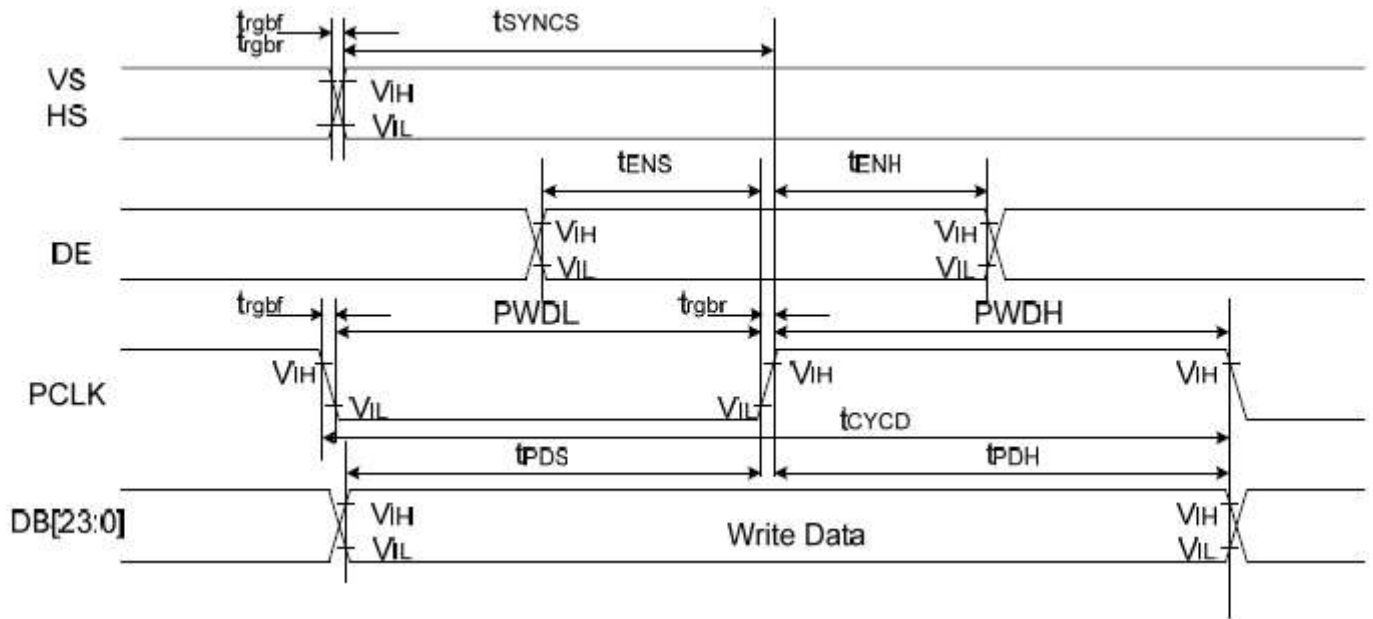


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	t <sub>css</sub>	Chip select time (Write)	15	-	ns	
	t <sub>csh</sub>	Chip select hold time (Read)	15	-	ns	
	t <sub>chw</sub>	CS "H" pulse width	40	-	ns	
SCL	t <sub>wc</sub>	Serial clock cycle (Write)	30	-	ns	
	t <sub>wrh</sub>	SCL "H" pulse width (Write)	10	-	ns	
	t <sub>wrl</sub>	SCL "L" pulse width (Write)	10	-	ns	
	t <sub>rc</sub>	Serial clock cycle (Read)	150	-	ns	
	t <sub>rdh</sub>	SCL "H" pulse width (Read)	60	-	ns	
	t <sub>rdl</sub>	SCL "L" pulse width (Read)	60	-	ns	
SDA/SDO (Output)	t <sub>acc</sub>	Access time (Read)	10	100	ns	For maximum CL=30pF
	t <sub>oh</sub>	Output disable time (Read)	15	100	ns	For minimum CL=8pF
SDA/SDI (Input)	t <sub>ds</sub>	Data setup time (Write)	10	-	ns	
	t <sub>dh</sub>	Data hold time (Write)	10	-	ns	

Note:

1. Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, T=10+/-0.5ns.
2. Does not include signal rise and fall times.

## 6.2 Parallel 24/18/16-bit RGB Interface Timing Characteristics

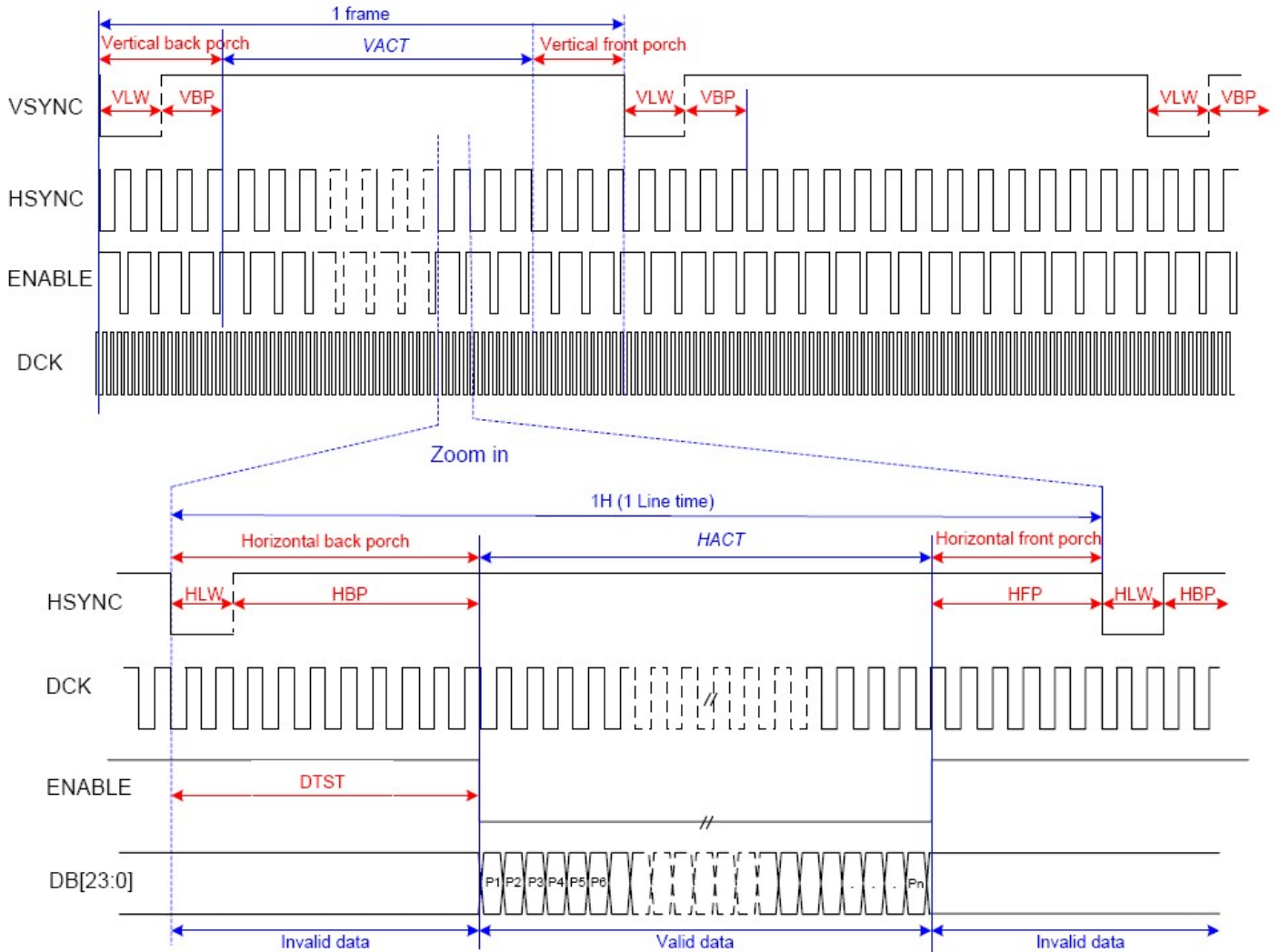


Signal	Symbol	Parameter	min	max	Unit	Description
VS/ HS	$t_{SYNCS}$	VS/HS setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	$t_{SYNCH}$	VS/HS hold time	5	-	ns	
DE	$t_{ENS}$	DE setup time	5	-	ns	
	$t_{ENH}$	DE hold time	5	-	ns	
DB[23:0]	$t_{POS}$	Data setup time	5	-	ns	
	$t_{PDH}$	Data hold time	5	-	ns	
PCLK	PWDH	PCLK high-level period	13	-	ns	
	PWDL	PCLK low-level period	13	-	ns	
	$t_{CYCD}$	PCLK cycle time	28	-	ns	
	$t_{rgbr}, t_{rgbf}$	PCLK,HS,VS rise/fall time	-	15	ns	

Note:  $T_a = -30$  to  $70$  °C,  $IOVCC=1.65V$  to  $3.6V$ ,  $VCI=2.5V$  to  $3.6V$ ,  $DGND=0V$

ISO9001

### 6.3 DPI Interface Timing



VLW : VSYNC Low pulse Width  
 HLW : HSYNC Low pulse Width  
 DTST : Data Transfer Startup Time  
 Pn : pixel 1, pixel 2..., pixel n.

Parameter	Symbols	Condition	Min.	Typ.	Max.	Units
Frame Rate	FR		54		66	fps
Horizontal Low Pulse width	HLW		1		-	DOTCLK
Horizontal Back Porch	HBP		2		126	DOTCLK
Horizontal Address	HACT			480		DOTCLK
Horizontal Front Porch	HFP		2		-	DOTCLK
Vertical Low Pulse width	VLW		1		126	Line
Vertical Back Porch	VBP		1		126	Line
Vertical Address	VACT				864	Line
Vertical Front Porch	VFP		1		255	Line
Data Clock	DCLK		16.6		41.7	MHz

## 6.4 Reset input timing

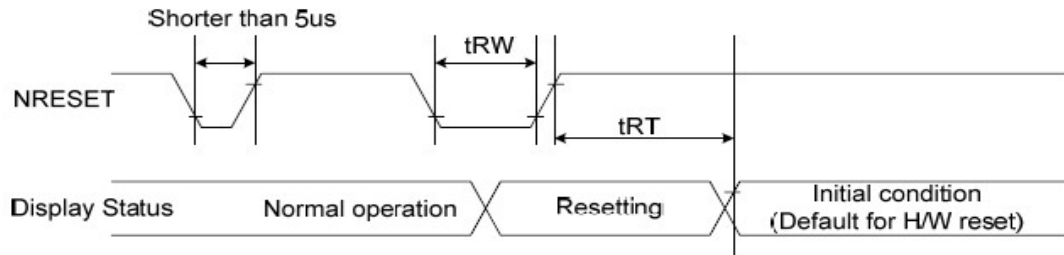


Figure 102 Reset Timing

Table 41 Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5(note 1,5) 120 (note 1,6,7)	ms

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from OTP to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 43.

Table 42 Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

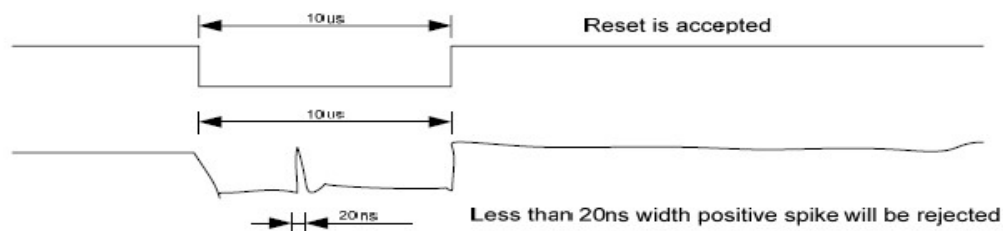


Figure 103 Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

## 7. CTP Specification

### 7.1 Electrical Characteristics

#### 7.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	2.66	3.47	V	--
Operating temperature	T <sub>OP</sub>	-40	+85	°C	--
Storage temperature	T <sub>ST</sub>	-60	+125	°C	--
Welding temperature (10s)	--	--	300	°C	--
ESD protection voltage (HB Model)	--	--	±2	KV	--

#### 7.1.2 DC Electrical Characteristics (Ta=25°C)

(Ambient temperature:25°C, AVDD=2.8V, VDDIO=1.8V or VDDIO=AVDD)

Item	Min.	Typ.	Max.	Unit	Note
Normal mode operating current	--	8	14.5	mA	
Green mode operating current	--	3.3	--	mA	
Sleep mode operating current	70	--	120	uA	
Doze mode operating current	--	0.78	--	mA	
Digital Input low voltage/VIL	-0.3	--	0.25*VDDIO	V	
Digital Input high voltage/VIH	0.75*VDDIO	--	VDDIO+0.3	V	
Digital Output low voltage/VOL	--		0.15*VDDIO	V	
Digital Output high voltage/VOH	0.85*VDDIO			V	

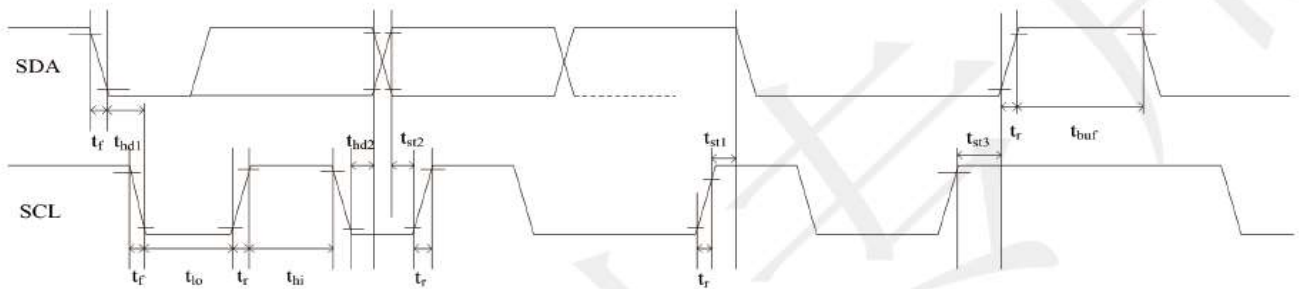
### 7.1.3 AC Characteristics

(Ambient temperature:25°C, AVDD=2.8V, VDDIO=1.8V)

Parameter	Min	Typ	Max	Unit
OSC oscillation frequency	59	60	61	MHZ
I/O output rise time,low to high	-	14	-	ns
I/O output rfall time,high to low	-	14	-	ns

### 7.2 I2C Timing

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:





**Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor**

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t <sub>lo</sub>	1.3	-	us
SCL high period	t <sub>hi</sub>	0.6	-	us
SCL setup time for Start condition	t <sub>st1</sub>	0.6	-	us
SCL setup time for Stop condition	t <sub>st3</sub>	0.6	-	us
SCL hold time for Start condition	t <sub>hd1</sub>	0.6	-	us
SDA setup time	t <sub>st2</sub>	0.1	-	us
SDA hold time	t <sub>hd2</sub>	0	-	us

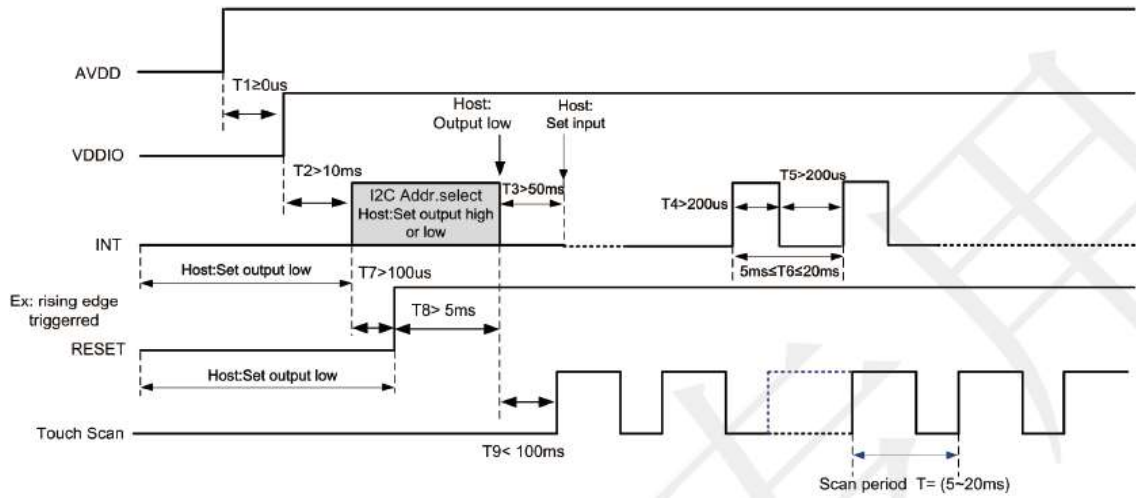
**Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor**

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t <sub>lo</sub>	1.3	-	us
SCL high period	t <sub>hi</sub>	0.6	-	us
SCL setup time for Start condition	t <sub>st1</sub>	0.6	-	us
SCL setup time for Stop condition	t <sub>st3</sub>	0.6	-	us
SCL hold time for Start condition	t <sub>hd1</sub>	0.6	-	us
SDA setup time	t <sub>st2</sub>	0.1	-	us
SDA hold time	t <sub>hd2</sub>	0	-	us

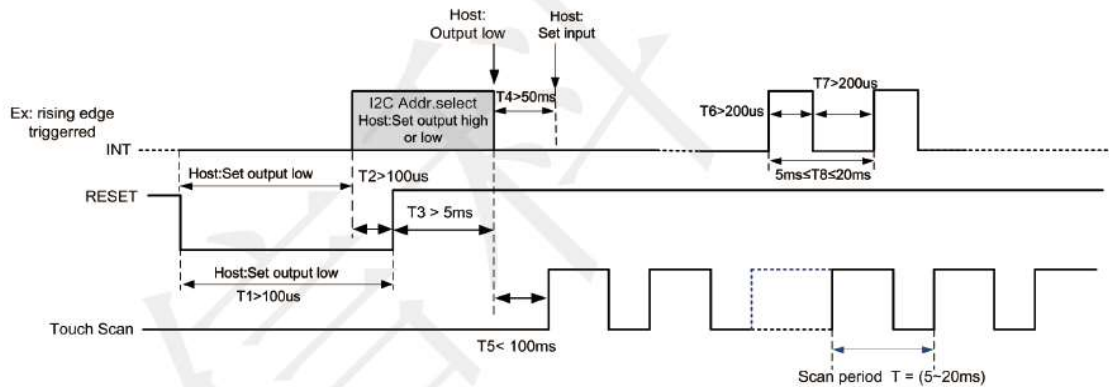
GT911 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timings:

ISO9001: 2008

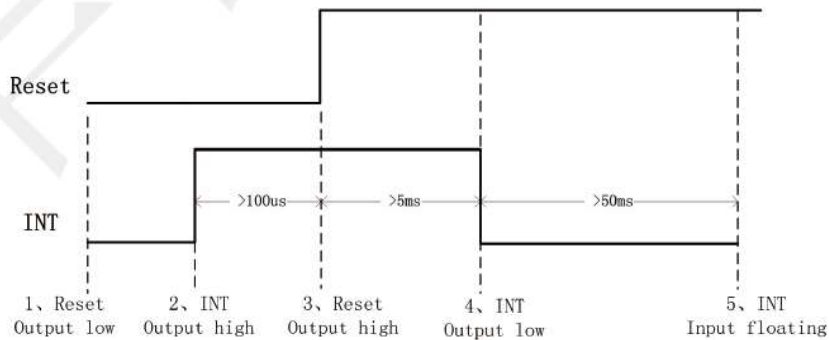
**Power-on Timing:**



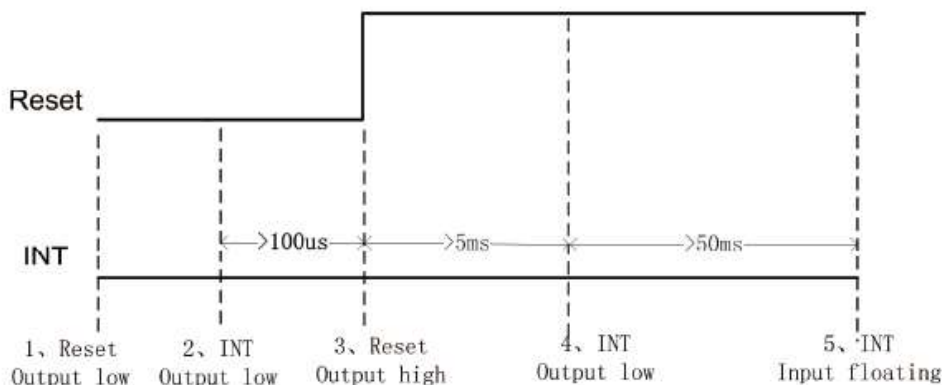
**Timing for host resetting GT911:**



**Timing for setting slave address to 0x28/0x29:**



**Timing for setting slave address to 0xBA/0xBB:**



**a) Data Transmission**

(For example: device address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from “high” to “low” when SCL line is “high”. Data flow or address is transmitted after the Start condition.

All slave devices connected to I<sup>2</sup>C bus should detect the 8-bit address issued after Start condition and send the correct ACK. After receiving matching address, GT911 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0XBA or 0XBB, GT911 will stay in an idle state.

For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is “high”.

When communication is completed, the host will issue the STOP condition. Stop condition implies the transition of SDA line from “low” to “high” when SCL line is “high”.

**b) Writing Data to GT911**

(For example: device address is 0xBA/0xBB)



**Timing for Write Operation**

The diagram above displays the timing sequence of the host writing data onto GT911. First, the host issues a Start condition. Then, the host sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation. Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

### c) Reading Data from GT911

(For example: device address is 0xBA/0xBB)



### Timing for Read Operation

The diagram above is the timing sequence of the host reading data from GT911. First, the host issues a Start condition and sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0xBB (Read Operation). After receiving ACK, the host starts to read data.

GT911 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

## 8. LCD Module Out-Going Quality Level

### 8.1 VISUAL & FUNCTION INSPECTION STANDARD

#### 8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

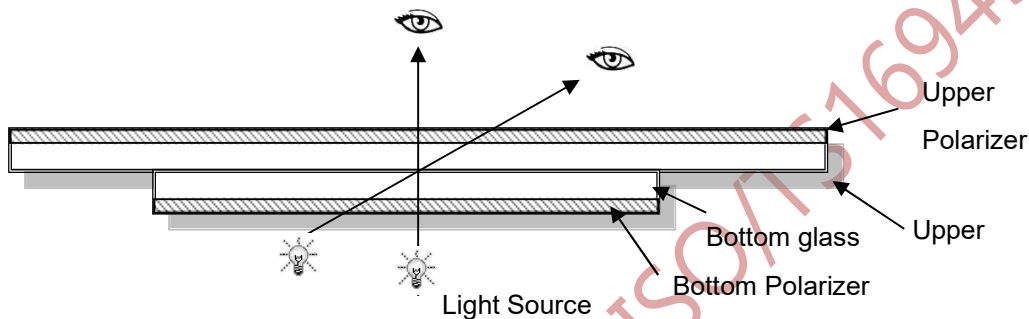
Temperature :  $25\pm 5^{\circ}\text{C}$

Humidity :  $65\%\pm 10\%\text{RH}$

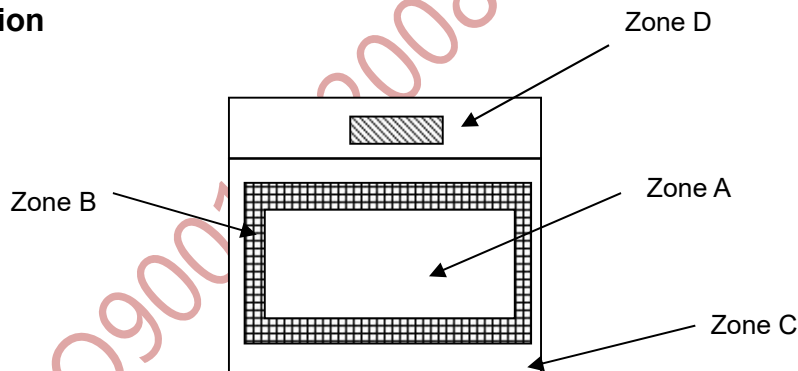
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



#### 8.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C Cover (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

Note: As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

### 8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

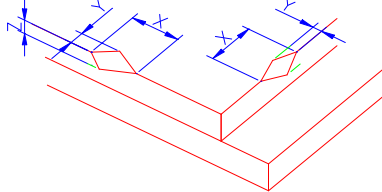
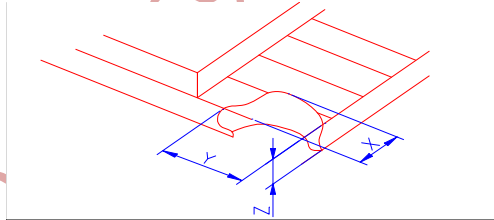
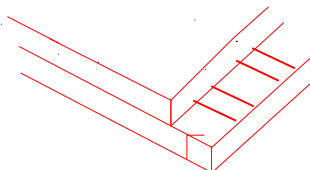
AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot Line defect	Light dot , Dim spot , Polarizer Bubble ; Polarizer accidented spot.	
6	Soldering appearance	Good soldering , Peeling off is not allowed.	
7	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

8.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of ITO, T: Height of LCD	(1) The edge of LCD broken	 <table border="1" data-bbox="754 667 1453 817"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤3.0mm</td> <td>&lt;Inner border line of the seal</td> <td>≤T</td> </tr> </tbody> </table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
X	Y	Z						
≤3.0mm	<Inner border line of the seal	≤T						
	(2)LCD corner broken	 <table border="1" data-bbox="813 1124 1394 1223"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤3.0mm</td> <td>≤L</td> <td>≤T</td> </tr> </tbody> </table>	X	Y	Z	≤3.0mm	≤L	≤T
X	Y	Z						
≤3.0mm	≤L	≤T						
	(3) LCD crack	 <p>Crack Not allowed</p>						

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ISC

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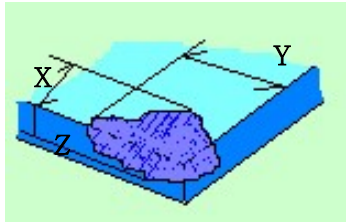
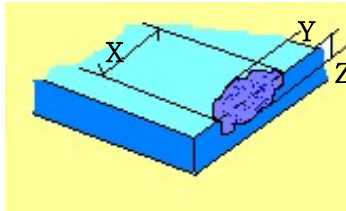


2.0	Spot defect	<p style="text-align: center;"><math>\Phi = (X+Y)/2</math></p>	① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)			
	Zone		Acceptable Qty			
	Size (mm)		A	B	C	
	$\Phi \leq 0.10$		Ignore			Ignore
	$0.10 < \Phi \leq 0.25$		3( distance $\geq 10\text{mm}$ )			
	$0.25 < \Phi \leq 0.3$		2			
	$\Phi > 0.35$		0			
	② Dim spot (LCD/TP/Polarizer dim dot, light leakage, dark spot)					
	Zone		Acceptable Qty			
	Size (mm)		A	B	C	
$\Phi \leq 0.1$	Ignore			Ignore		
$0.10 < \Phi \leq 0.25$	3( distance $\geq 10\text{mm}$ )					
$0.25 < \Phi \leq 0.3$	2					
$\Phi > 0.35$	0					
③ Polarizer accidented spot						
Zone		Acceptable Qty				
Size (mm)	A	B	C			
$\Phi \leq 0.2$	Ignore			Ignore		
$0.3 < \Phi \leq 0.5$	2( distance $\geq 10\text{mm}$ )					
$\Phi > 0.5$	0					
④ Pixel bad points (light dot, Dim dot, color dot)						
Zone		Acceptable Qty				
Size (mm)	A	B	C			
$\Phi \leq 0.1$	Ignore			Ignore		
$0.15 < \Phi \leq 0.25$	2( distance $\geq 10\text{mm}$ )					
$\Phi > 0.3$	0					
⑤ Polarizer Bubble						
Zone		Acceptable Qty				
Size (mm)	A	B	C			
$\Phi \leq 0.2$	Ignore			Ignore		
$0.3 < \Phi \leq 0.4$	3(distance $\geq 10\text{mm}$ )					
$0.5 < \Phi \leq 0.6$	2					
$0.6 < \Phi$	0					

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3.0	Line defect (LCD/TP /Polarizer backlight black/white line, scratch, stain)	<table border="1"> <tr> <th rowspan="2">Width(mm)</th> <th rowspan="2">Length(m) m)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> <tr> <td><math>\Phi \leq 0.05</math></td> <td>Ignore</td> <td colspan="3">Ignore</td> </tr> <tr> <td><math>0.05 &lt; W \leq 0.06</math></td> <td><math>L \leq 4.0</math></td> <td colspan="3">N<math>\leq</math>3</td> </tr> <tr> <td><math>0.07 &lt; W \leq 0.08</math></td> <td><math>L \leq 3.0</math></td> <td colspan="3">N<math>\leq</math>2</td> </tr> <tr> <td><math>0.08 &lt; W</math></td> <td colspan="4">Define as spot defect</td> </tr> </table>	Width(mm)	Length(m) m)	Acceptable Qty			A	B	C	$\Phi \leq 0.05$	Ignore	Ignore			$0.05 < W \leq 0.06$	$L \leq 4.0$	N $\leq$ 3			$0.07 < W \leq 0.08$	$L \leq 3.0$	N $\leq$ 2			$0.08 < W$	Define as spot defect				Ignore
		Width(mm)			Length(m) m)	Acceptable Qty																									
			A	B		C																									
		$\Phi \leq 0.05$	Ignore	Ignore																											
		$0.05 < W \leq 0.06$	$L \leq 4.0$	N $\leq$ 3																											
$0.07 < W \leq 0.08$	$L \leq 3.0$	N $\leq$ 2																													
$0.08 < W$	Define as spot defect																														
4.0	Electronic Components SMT	Not allow missing parts, solderless connection, cold solder joint, mismatch, The positive and negative polarity opposite																													
5.0	Display color & Brightness	<p>1. Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples.</p> <p>2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</p>																													
6.0	LCD Mura	By 5% ND filter invisible.																													

7.0	CTP Related	CTP Cover sensor accidented black/white spot	<table border="1"> <tr> <th rowspan="2">Size <math>\Phi</math>(mm)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> <tr> <td><math>\Phi \leq 0.1</math></td> <td colspan="3">Ignore</td> </tr> <tr> <td><math>0.1 &lt; \Phi \leq 0.2</math></td> <td colspan="3">3 (distance <math>\geq</math> 10mm)</td> </tr> <tr> <td><math>0.20 &lt; \Phi \leq 0.25</math></td> <td colspan="3">2</td> </tr> <tr> <td><math>\Phi &gt; 0.3</math></td> <td colspan="3">0</td> </tr> </table>	Size $\Phi$ (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.1$	Ignore			$0.1 < \Phi \leq 0.2$	3 (distance $\geq$ 10mm)			$0.20 < \Phi \leq 0.25$	2			$\Phi > 0.3$	0			Ignore		
		Size $\Phi$ (mm)	Acceptable Qty																										
A	B		C																										
$\Phi \leq 0.1$	Ignore																												
$0.1 < \Phi \leq 0.2$	3 (distance $\geq$ 10mm)																												
$0.20 < \Phi \leq 0.25$	2																												
$\Phi > 0.3$	0																												
CTP Cover scratch	<table border="1"> <tr> <th rowspan="2">Width(mm)</th> <th rowspan="2">Ignore(mm)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> <tr> <td><math>\Phi \leq 0.05</math></td> <td>Ignore</td> <td colspan="3">Ignore</td> </tr> <tr> <td><math>0.05 &lt; W \leq 0.06</math></td> <td><math>L \leq 4.0</math></td> <td colspan="3">N<math>\leq</math>3</td> </tr> <tr> <td><math>0.07 &lt; W \leq 0.08</math></td> <td><math>L \leq 3.0</math></td> <td colspan="3">N<math>\leq</math>2</td> </tr> <tr> <td><math>0.08 &lt; W</math></td> <td colspan="4">Define as spot defect</td> </tr> </table>	Width(mm)	Ignore(mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.05$	Ignore	Ignore			$0.05 < W \leq 0.06$	$L \leq 4.0$	N $\leq$ 3			$0.07 < W \leq 0.08$	$L \leq 3.0$	N $\leq$ 2			$0.08 < W$	Define as spot defect			
Width(mm)	Ignore(mm)			Acceptable Qty																									
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$0.07 < W \leq 0.08$	$L \leq 3.0$	N $\leq$ 2																											
$0.08 < W$	Define as spot defect																												

		CTP Cover Pinhole/ Lack of ink	<table border="1"> <tr> <th rowspan="2">Zone Size (mm)</th> <th>Acceptable Qty</th> </tr> <tr> <th>C</th> </tr> <tr> <td><math>\Phi \leq 0.1</math></td> <td>Ignore</td> </tr> <tr> <td><math>0.1 &lt; \Phi \leq 0.2</math></td> <td>3(distance <math>\geq 10</math>mm)</td> </tr> <tr> <td><math>0.25 &lt; \Phi \leq 0.3</math></td> <td>2</td> </tr> <tr> <td><math>\Phi &gt; 0.35</math></td> <td>0</td> </tr> </table>		Zone Size (mm)	Acceptable Qty	C	$\Phi \leq 0.1$	Ignore	$0.1 < \Phi \leq 0.2$	3(distance $\geq 10$ mm)	$0.25 < \Phi \leq 0.3$	2	$\Phi > 0.35$	0				
			Zone Size (mm)	Acceptable Qty															
				C															
			$\Phi \leq 0.1$	Ignore															
$0.1 < \Phi \leq 0.2$	3(distance $\geq 10$ mm)																		
$0.25 < \Phi \leq 0.3$	2																		
$\Phi > 0.35$	0																		
CTP Bonding bubble/ accidented spot	<table border="1"> <tr> <th rowspan="2">Size <math>\Phi</math>(mm)</th> <th colspan="2">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> </tr> <tr> <td><math>\Phi \leq 0.1</math></td> <td colspan="2">Ignore</td> </tr> <tr> <td><math>0.15 &lt; \Phi \leq 0.2</math></td> <td colspan="2">3(distance <math>\geq 10</math>mm)</td> </tr> <tr> <td><math>0.2 &lt; \Phi \leq 0.25</math></td> <td colspan="2">2</td> </tr> <tr> <td><math>\Phi &gt; 0.25</math></td> <td colspan="2">0</td> </tr> </table>		Size $\Phi$ (mm)	Acceptable Qty		A	B	$\Phi \leq 0.1$	Ignore		$0.15 < \Phi \leq 0.2$	3(distance $\geq 10$ mm)		$0.2 < \Phi \leq 0.25$	2		$\Phi > 0.25$	0	
	Size $\Phi$ (mm)	Acceptable Qty																	
		A	B																
	$\Phi \leq 0.1$	Ignore																	
$0.15 < \Phi \leq 0.2$	3(distance $\geq 10$ mm)																		
$0.2 < \Phi \leq 0.25$	2																		
$\Phi > 0.25$	0																		
Assembly deflection	beyond the edge of backlight $\leq 0.2$ mm																		
TP cover broken X : length Y : width Z : height	<table border="1"> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> <tr> <td><math>X \leq 0.5</math>mm</td> <td><math>Y \leq 0.5</math>mm</td> <td>Z &lt; cover thicknes s</td> </tr> </table> <p>* Circuitry broken is not allowed.</p>	X	Y	Z	$X \leq 0.5$ mm	$Y \leq 0.5$ mm	Z < cover thicknes s												
X	Y	Z																	
$X \leq 0.5$ mm	$Y \leq 0.5$ mm	Z < cover thicknes s																	
TP cover broken X : length Y : width Z : height	<table border="1"> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> <tr> <td><math>X \leq 0.3</math>mm</td> <td><math>Y \leq 0.3</math>mm</td> <td>Z &lt; LCD thicknes s</td> </tr> </table> <p>* Circuitry broken is not allowed.</p>	X	Y	Z	$X \leq 0.3$ mm	$Y \leq 0.3$ mm	Z < LCD thicknes s												
X	Y	Z																	
$X \leq 0.3$ mm	$Y \leq 0.3$ mm	Z < LCD thicknes s																	

Criteria ( functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

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## 9. Reliability Test Result

### 9.1 Condition

Item	Condition	Inspection after test
High Temperature Operating	70℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20℃, 96HR	
High Temperature Storage	80℃, 96HR	
Low Temperature Storage	-30℃, 96HR	
High Temperature & High Humidity Operating	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-30℃,30 min ↔ 80℃,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM BOX)	

Remark:

- 1.The test samples should be applied to only one test item.
- 2.Sample size for each test item is 5~10pcs.
- 3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.
- 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

Part. No	KD050FWFPA011-C009A	REV	V1.2	Page 31 of 33
	常备库存 Standing Stock	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range

## 10. Cautions and Handling Precautions

### 10.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.  
Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.  
If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.  
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

### 10.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.  
It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.  
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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	常备库存 Standing Stock	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range

## 11. Packing

----TBD-----

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Part. No	KD050FWFPA011-C009A	REV	V1.2	Page 33 of 33
	常备库存 Standing Stock	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range