Product Specification

To:

Product Name: RM133NWF4 RC

Document Issue Date: 2022/10/14

Note: 1. Please contact * * * Company. before designing your product based on this product.
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by CH for any intellectual property claims or other problems that may result from application based on the module described herein.

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1.0 General Descriptions

1.1 Introduction

The CD21119-01 is a Color Active Matrix Liquid Crystal Display with a light system. The matrix uses a-Si Thin Film Transistor as a switching device. This TFT LCD has a 13.3 inch diagonally measured active display area with FHD resolution (1, 920 horizontal by 1,080 vertical pixels array).

1.2 Features

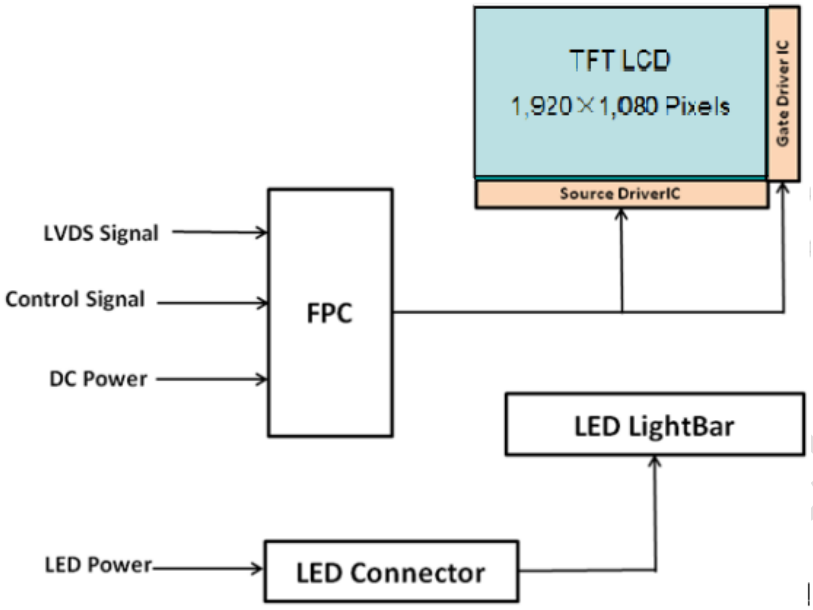
- ■ Supported FHD Resolution
- ■ eDP Interface
- ■ Wide View Angle
- ■ Compatible with RoHS Standard

1.3 Product Summary

Items		Specifications	Unit
Screen Diagonal		13.3	inch
Active Area (H x V)		293.76×165.24	mm
Number of Pixels (H x V)		1,920 x 1,080	-
Pixel Pitch (H x V)		0.1530 x 0.1530	mm
Pixel Arrangement		R.G.B. Vertical Stripe	-
Display Mode		Normally Black	-
White Luminance		1000 (Typ.)	cd /m^2
Contrast Ratio		1200 (Typ.)	-
Response Time		30 (Typ.)	ms
Input Voltage		3.3 (Typ.)	V
Power Consumption		3.7(Max.) @Mosaic Pattern	W
Weight		390 (Max.)	g
Outline Dimension (H x V x D)	PCB side	307.60(Typ.) x 183.05 (Typ.) x 7.28(Max.)	mm
	LCD side	307.60(Typ.) x 183.05 (Typ.) x 5.50(Max.)	mm
Electrical Interface (Logic)		eDP	-
Support Color		6bit+FHRC	
-NTSC		72(Typ.)	%
Viewing Direction		All	-
Surface Treatment		AG	-

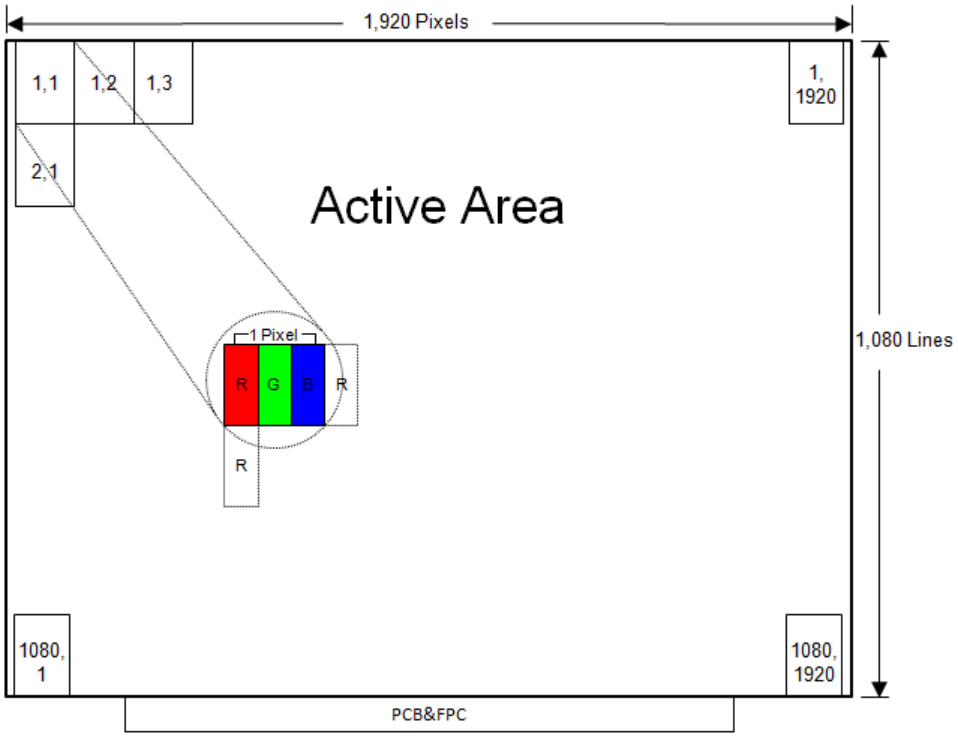
1.4 Functional Block Diagram

Figure 1 shows the functional block diagram of the LCD module.



1.5 Pixel Mapping

Figure2 Pixel Mapping



2.0 Absolute Maximum Ratings

Table 1 Electrical & Environment Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Logic Supply Voltage	V_{DD}	-0.3	3.6	V	(1),(2),(3),(4)
Logic Input Signal Voltage	V_{Signal}	0.2	0.4	V	
Operating Temperature	T_{gs}	0	50	℃	
Storage Temperature	T_a	-20	60	℃	

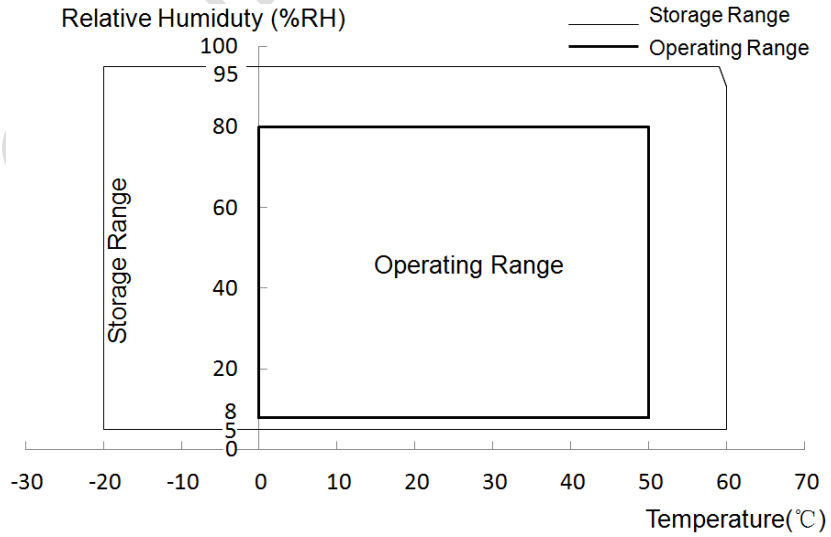
Note (1) All the parameters specified in the table are absolute maximum rating values that may cause faulty operation or unrecoverable damage, if exceeded. It is recommended to follow the typical value.

Note (2) All the contents of electro-optical specifications and display fineness are guaranteed under Normal Conditions. All the display fineness should be inspected under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH.

Note (3) Unpredictable results may occur when it was used in extreme conditions. T_a= Ambient Temperature, T_{gs}= Glass Surface Temperature. All the display fineness should be inspected under normal conditions.

Note (4) Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be lower than 46℃, and no condensation of water. Besides, protect the module from static electricity.

Figure 3 Absolute Ratings of Environment of the LCD Module



3.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

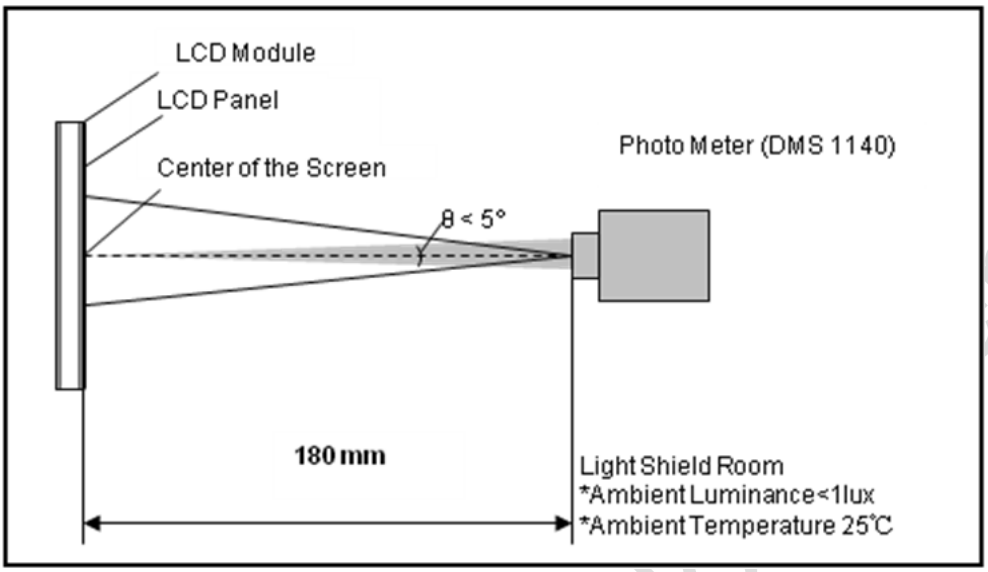
Table 2 Optical Characteristics

Item	Conditions		Min.	Typ.	Max.	Unit	Note
Viewing Angle （CR≥10）	Horizontal	θ_{x+}	80	85	-	degree	(1),(2),(3),(4),(8)
		θ_{x-}	80	85	-		
	Vertical	θ_{y+}	80	85	-		
		θ_{y-}	80	85	-		
Contrast Ratio	Center		1,000	1,200	-	-	(1),(2),(4),(8) θx=θy=0°
Response Time	Rising + Falling		-	30	35	ms	(1),(2),(5),(8) θx=θy=0°
Color Chromaticity (CIE1931)	Red x		Typ. -0.03	0.628	Typ. +0.03	-	(1),(2),(3),(8) θx=θy=0°
	Red y			0.341		-	
	Green x			0.339		-	
	Green y			0.549		-	
	Blue x			0.110		-	
	Blue y			0.089		-	
	White x			0.306		-	
	White y			0.343		-	
NTSC	-		72	-	-	%	(1),(2),(3),(8) θx=θy=0°
White Luminance	5 Points Average		-	1000	-	cd/m^2	(1),(2),(6),(8) θx=θy=0°
Luminance Uniformity	5 Points		80	-	-	%	(1),(2),(7),(8) θx=θy=0°
	13 Points		60	-	-		

Note (1) Measurement Setup:

The LCD module should be stabilized at given ambient temperature (25℃) for 30 minutes to avoid abrupt temperature changing during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 30 minutes in the windless room.

Figure 4 Measurement Setup



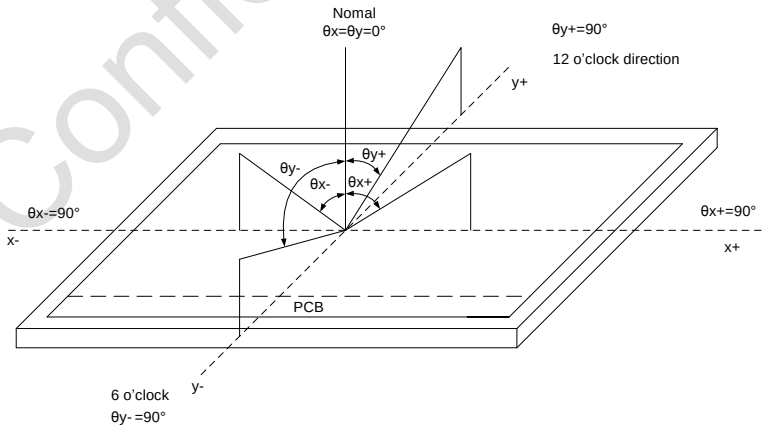
Note (2) The LED input parameter setting as:

V_{LED} =10.5V

PWM_LED: Duty 100%

Note (3) Definition of Viewing Angle

Figure 5 Definition of Viewing Angle



Note (4) Definition of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression:

Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255, L0: Luminance of gray level 0

Note (5) Definition of Response Time (T_R, T_F)

Figure 6 Definition of Response Time

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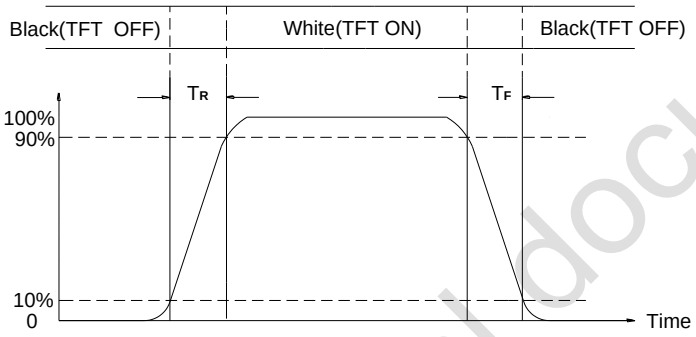


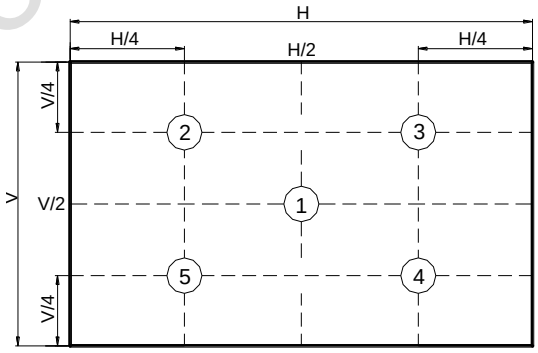
Note (6) Definition of Luminance White

Measure the luminance of gray level 255 (Ref.: Active Area)

Display Luminance=(L1+L2+L3+L4+L5) / 5

H—Active Area Width, V—Active Area Height, L—Luminance

Figure 7 Measurement Locations of 5 Points



Note (7) Definition of Luminance Uniformity (Ref.: Active Area)

Measure the luminance of gray level 255 at 5 points.

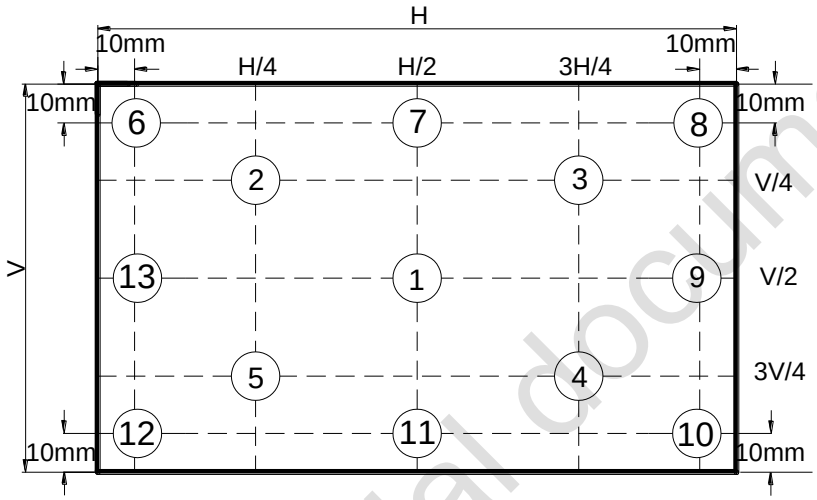
Luminance Uniformity= Min.(L1, L2, ... L5) / Max.(L1, L2, ... L5)

Measure the luminance of gray level 255 at 13 points.

Luminance Uniformity= Min.(L1, L2, ... L13) / Max.(L1, L2, ... L13)

H—Active Area Width, V—Active Area Height, L—Luminance

Figure 8 Measurement Locations of 13 Points



Note (8) All optical data based on CH given system & nominal parameter & testing machine in this document.

4.0 Electrical Characteristics

4.1 Interface Connector

Table 3 Signal Connector Type

Item	Description
Manufacturer / Type	IPEX 20455-030E

Table 4 Signal Connector Pin Assignment

Pin No.	Symbol	Description	Remarks
1	NC Reserved	Reserved for LCD manufacturer's use	-
2	GND	High Speed Ground	-
3	Lane1_N	Complement Signal Link Lane 1	-
4	Lane1_P	True Signal Link Lane 1	-
5	GND	High Speed Ground	-
6	Lane0_N	Complement Signal Link Lane 0	-
7	Lane0_P	True Signal Link Lane 0	-
8	GND	High Speed Ground	-
9	AUX_CH_P	True Signal Auxiliary Channel	-
10	AUX_CH_N	Complement Signal Auxiliary Channel	-
11	GND	High Speed Ground	-
12	VDD	LCD logic and driver power	-
13	VDD	LCD logic and driver power	-
14	NC	LCD Panel Self Test Enable	-
15	GND	LCD logic and driver ground	-
16	GND	LCD logic and driver ground	-
17	HPD	HPD signal pin	-
18	NC Reserved	Reserved for LCD manufacturer's use	-
19	NC Reserved	Reserved for LCD manufacturer's use	-
20	NC Reserved	Reserved for LCD manufacturer's use	-
21	NC Reserved	Reserved for LCD manufacturer's use	-
22	NC Reserved	Reserved for LCD manufacturer's use	-
23	NC Reserved	Reserved for LCD manufacturer's use	-
24	NC Reserved	Reserved for LCD manufacturer's use	-
25	NC Reserved	Reserved for LCD manufacturer's use	-
26	NC Reserved	Reserved for LCD manufacturer's use	-
27	NC Reserved	Reserved for LCD manufacturer's use	-
28	NC Reserved	Reserved for LCD manufacturer's use	-

29	NC Reserved	Reserved for LCD manufacturer's use	-
30	NC Reserved	Reserved for LCD manufacturer's use	-

4.2 Signal Electrical Characteristics

Table 5 Display Port Main Link

Parameter	Description	Min.	Typ.	Max.	Unit
V_{CM}	Differentia Common Mode Voltage	0	-	2.0	V
$V_{Diff\ P-P}$ Level 1	Differential Peak to Peak Voltage Level 1	0.34	0.40	0.46	V
$V_{Diff\ P-P}$ Level 2	Differential Peak to Peak Voltage Level 2	0.51	0.60	0.68	V
$V_{Diff\ P-P}$ Level 3	Differential Peak to Peak Voltage Level 3	0.69	0.80	0.92	V
$V_{Diff\ P-P}$ Level 4	Differential Peak to Peak Voltage Level 4	1.02	1.20	1.38	V

Note: (1) Input signals shall be low or Hi- resistance state when VDD is off.

(2) It is recommended to refer the specifications of VESA Display Port Standard V1.2 in detail.

(3) Follow as VESA display port standard V1.2 at both 1.62 and 2.7Gbps link rates.

Figure 9 Display Port Main Link Signal

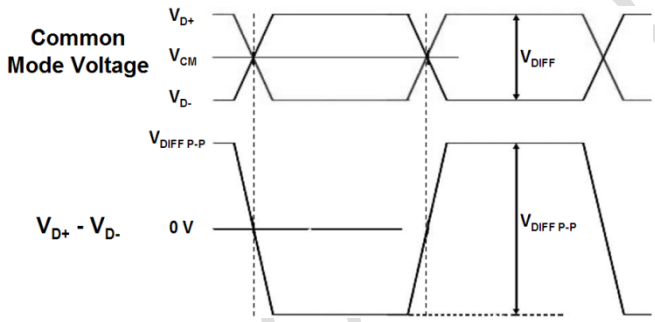


Figure10 Display Port AUX_CH Signal

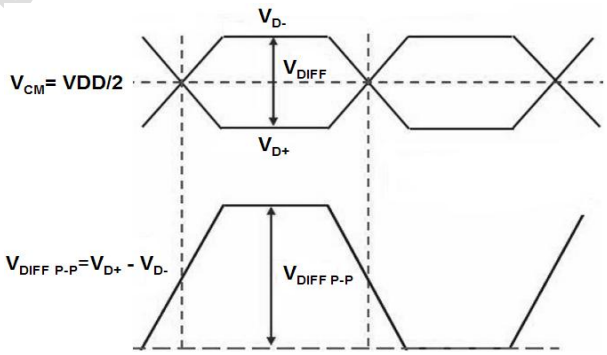


Table 6 Display Port AUX_CH

Parameter	Description	Min.	Typ.	Max.	Unit
V_{CM}	Differentia Common Mode Voltage	0	VDD/2	2	V
$V_{Diff\ P-P}$	Differential Peak to Peak Voltage	0.39	-	1.38	V

Note: Follow as VESA display port standard V1.2.

Table 7 Display Port V_{HPD}

Parameter	Description	Min.	Typ.	Max.	Unit

V_{HPD}	HPD Voltage	2.25	-	3.60	V

Note: Follow as VESA display port standard V1.2.

4.3 Interface Timings

Table 8 Interface Timings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock Frequency	Fclk	87.9	138.5	148.5	MHz
H Total Time	HT	2020	2080	3900	Clocks
H Active Time	HA		1,920		Clocks
V Total Time	VT	1090	1111	2046	Lines
V Active Time	VA		1,080		Lines
Frame Rate	FV	48	60	65	Hz

Note (1): HT*VT*FV<148.5MHz

Note (2): All reliabilities are specified for timing specification based on refresh rate of 60Hz. However, CD21119-01(H) has a good actual performance even at lower refresh rate (e.g. 48Hz) for power saving mode, whereas CD21119-01(H) is secured only for function under lower refresh rate; 60Hz at Normal mode, 48Hz at Power save mode.

4.4 Input Power Specifications

Input power specifications are as follows.

Table 9 Input Power Specifications

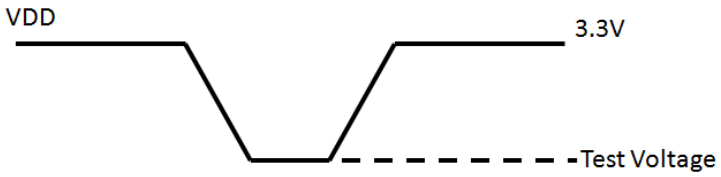
Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
System Power Supply							
LCD Drive Voltage (Logic)		V_{DD}	3	3.3	3.6	V	(1),(2),(3)
VDD Current	Mosaic Pattern	I_{DD}	-	-	0.27	A	(1),(4)
VDD Power Consumption	Mosaic Pattern	P_{DD}	-	-	0.89	W	
Rush Current		I_{Rush}	-	-	1.5	A	(1),(5)
Allowable Logic/LCD Drive Ripple Voltage		V_{VDD-RP}	-	-	200	mV	(1)
LED Power Supply							
LED Input Voltage		V_{LED}	-	-	18	V	(1),(2)
LED Power Consumption		P_{LED}	5.9	-	6.5	W	(1),(6)
LED Forward Voltage		V_F	-	-	3.0	V	(1),(2)
LED Forward Current		I_F	-	360	-	mA	
LED Life Time		LT	15,000	25,000	-	Hours	(1),(7)

Note (1) All of the specifications are guaranteed under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH.

Note (2) All of the absolute maximum ratings specified in the table, if exceeded, may cause faulty operation or unrecoverable damage. It is recommended to follow the typical value.

Note (3) VDD Power Dip Condition for Lenovo.

Figure 11 VDD Power Dip



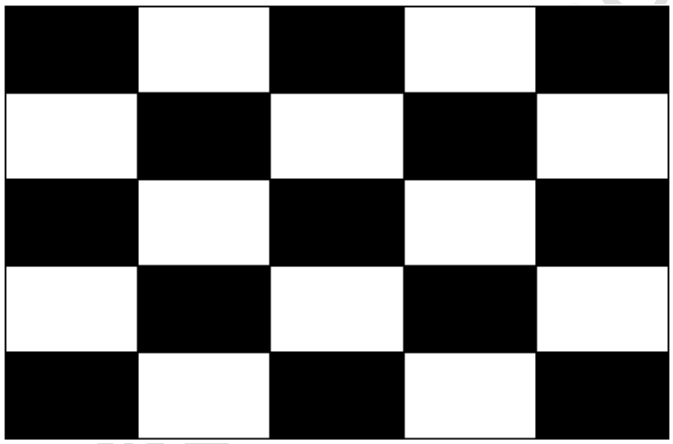
Test criteria:

1) 2.4≤Test Voltage≤3.3V: Normal operation

2) 2.0V≤Test Voltage＜2.4V: No abnormal display after back to 3.3V input.

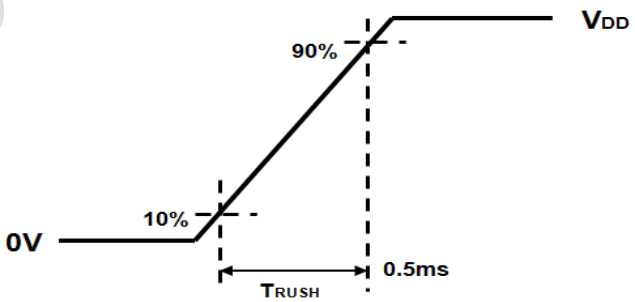
Note (4) The specified V_{DD} current and power consumption are measured under the V_{DD} = 3.3 V, F_V = 60 Hz condition and Mosaic Pattern.

Figure 12 Mosaic pattern



Note (5) The figures below is the measuring condition of V_{DD}. Rush current can be measured when T_{RUSH} is 0.5 ms.

Figure 13 V_{DD} Rising Time



Note (6) The power consumption of LED Driver are under the V_{LED} = 12.0V, Dimming of Max luminance.

Note (7) The life time is determined as the sum of the lighting time till the luminance of LCD at the typical LED current reducing to 50% of the minimum value under normal operating condition.

4.5 Power ON/OFF Sequence

Interface signals are also shown in the chart. Signals from any system shall be Hi- resistance state or low level when VDD voltage is off.

Figure 14 Power Sequence

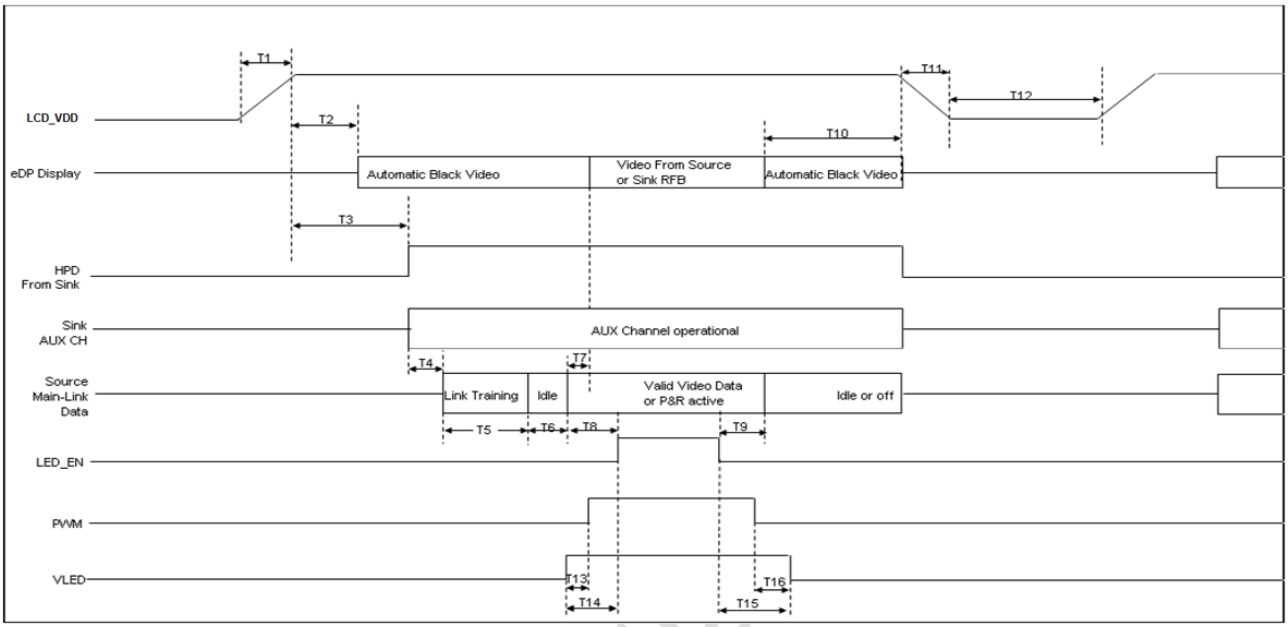


Table 10 Power Sequencing Requirements

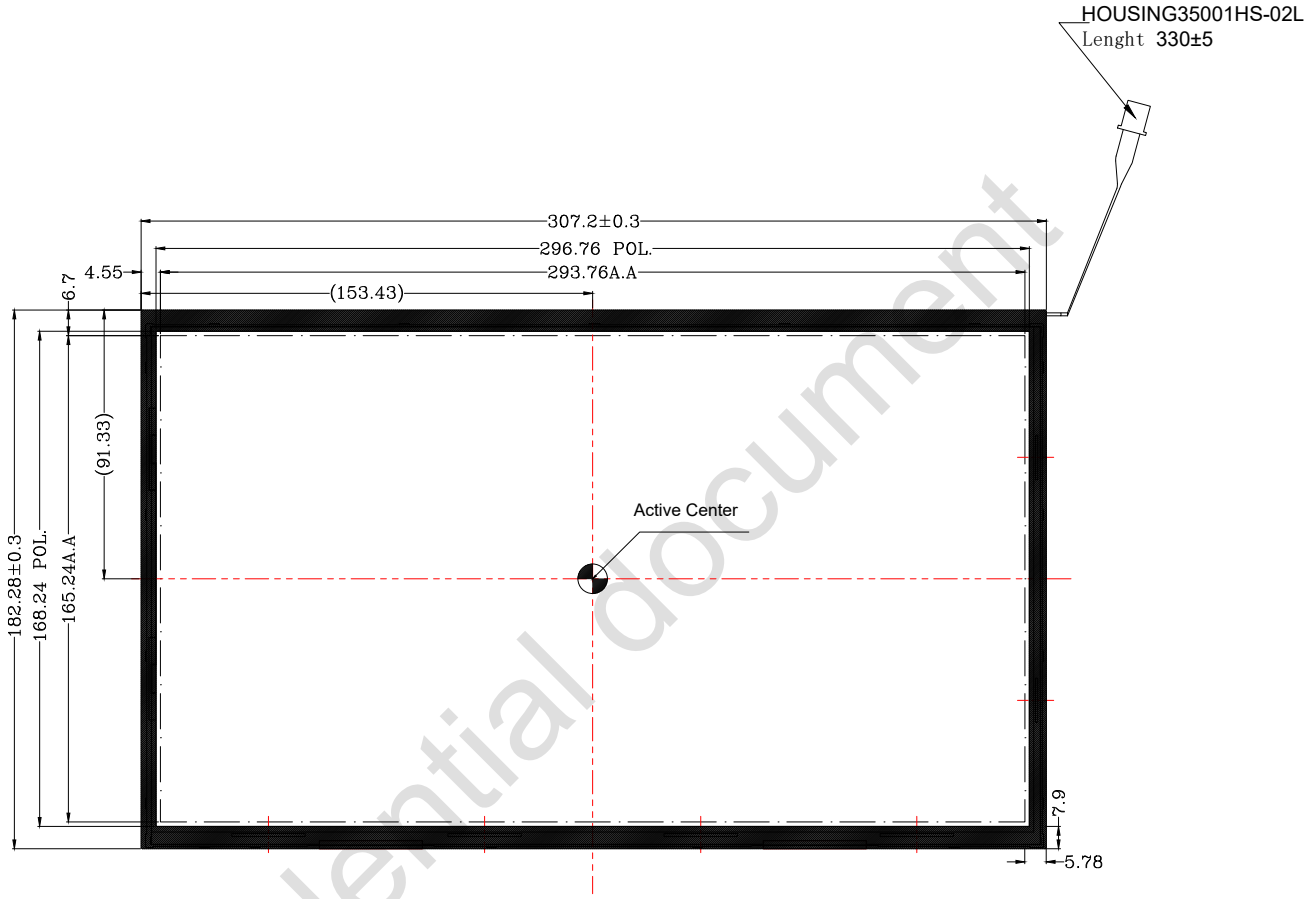
Parameter	Symbol	Min.	Typ.	Max.	Unit
VDD Rise Time (10% to 90%)	T1	0.5	-	10	ms
Delay from VDD to automatic Black Video generation	T2	0	-	200	ms
Delay from VDD to HPD high	T3	0	-	200	ms
Delay from HPD high to link training initialization	T4	-	-	-	ms
Link training duration	T5	-	-	-	ms
Link idle	T6	-	-	-	ms
Delay from valid video data from Source to video on display	T7	0	-	50	ms
Delay from valid video data from Source to backlight enable	T8	-	-	-	ms
Delay from backlight disable to end of valid video date	T9	-	-	-	ms
Delay from end of valid video data from Source to VDD off	T10	0	-	500	ms
VDD fall time (90% to 10%)	T11	0	-	10	ms
VDD off time	T12	500	-	-	ms
Delay from VLED to PWM	T13	0	-	-	ms
Delay from VLED to backlight enable	T14	0	-	-	ms

Delay from backlight disable to VLED off	T15	0	-	-	ms
Delay from PWM off to VLED off	T16	0	-	-	ms

5.0 Mechanical Characteristics

5.1 Outline Drawing

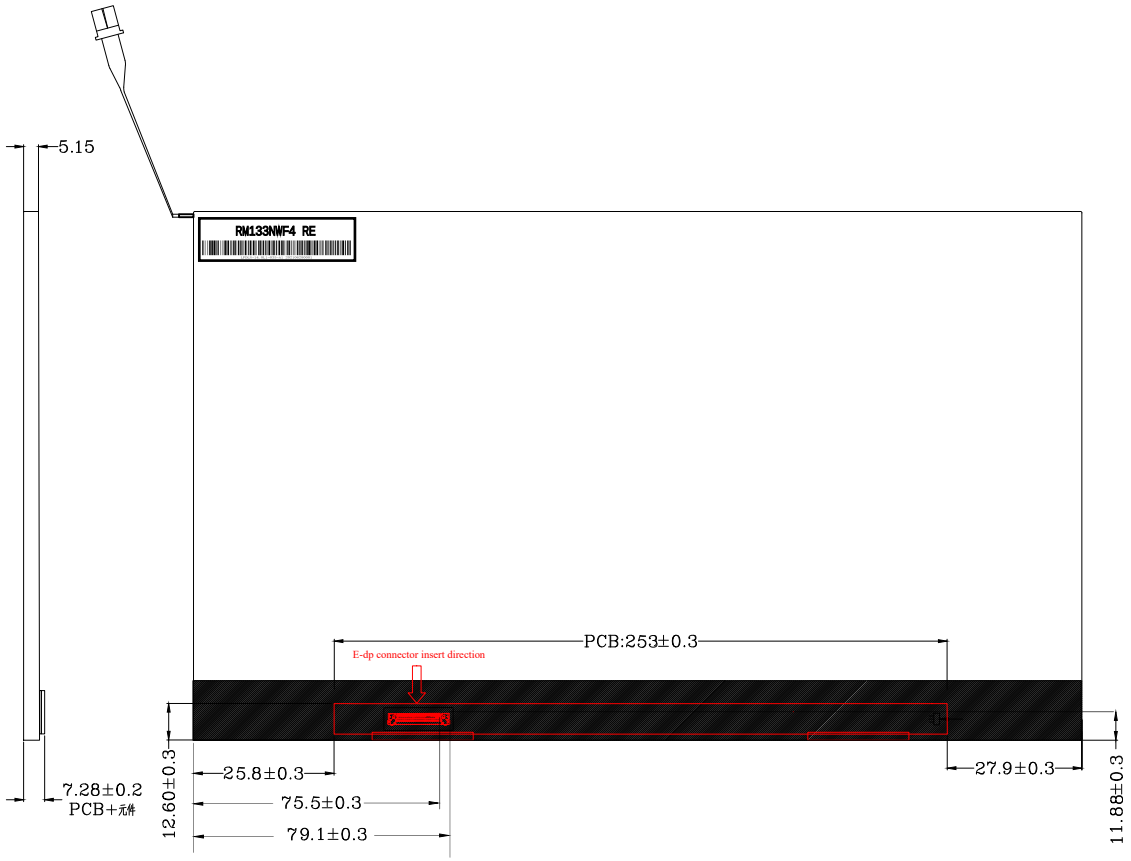
Figure 15 Reference Outline Drawing (Front Side)



5.0 Mechanical Characteristics

5.1 Outline Drawing

Figure 15 Reference Outline Drawing (Back Side)



6.0 Reliability Conditions

Table 12 Reliability Condition

Item		Package	Test Conditions		Note
High Temperature/High Humidity Operating Test		Module	T_{gs}=(50℃, 80%RH, 1000 hours)		(1),(2),(3),(4)
Low Temperature Operating Test		Module	T_a=0℃, 500 hours		
High Temperature Storage Test		Module	T_a=60℃, 240 hours		(1),(3),(4)
Low Temperature Storage Test		Module	T_a=-20℃, 240 hours		
Shock Non-operating Test		Module	210G, 3ms half-sine ±x ±y ±z each aixs/1times 50G, 18msec Trapezoidal ±x ±y ±z each aixs/1times		(1),(3),(5)
Vibration Non-operating Test		Module	1.5G , 10~200 Hz , x、y、z each axis/30min.		
ESD Test	Operating	Module	Contact	±8KV, 150pF(330Ohm)	(1),(2),(6)
			Air	±15KV, 150pF(330Ohm)	

Note (1) A sample can only have one test. Outward appearance, image quality and optical data can only be checked at normal conditions according to the CH document before reliable test. Only check the function of the module after reliability test.

Note (2) The setting of electrical parameters should follow the typical value before reliability test.

Note (3) During the test, it is unaccepted to have condensate water remains. Besides, protect the module from static electricity.

Note (4) The sample must be released for 24 hours under normal conditions before judging. Furthermore, all the judgment must be made under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH. T_a= Ambient Temperature, T_{gs}= Glass Surface Temperature.

Note (5) The module should be fixed firmly in order to avoid twisting and bending.

Note (6) It could be regarded as pass, when the module recovers from function fault caused by ESD after resetting.

8.0 Package Specification

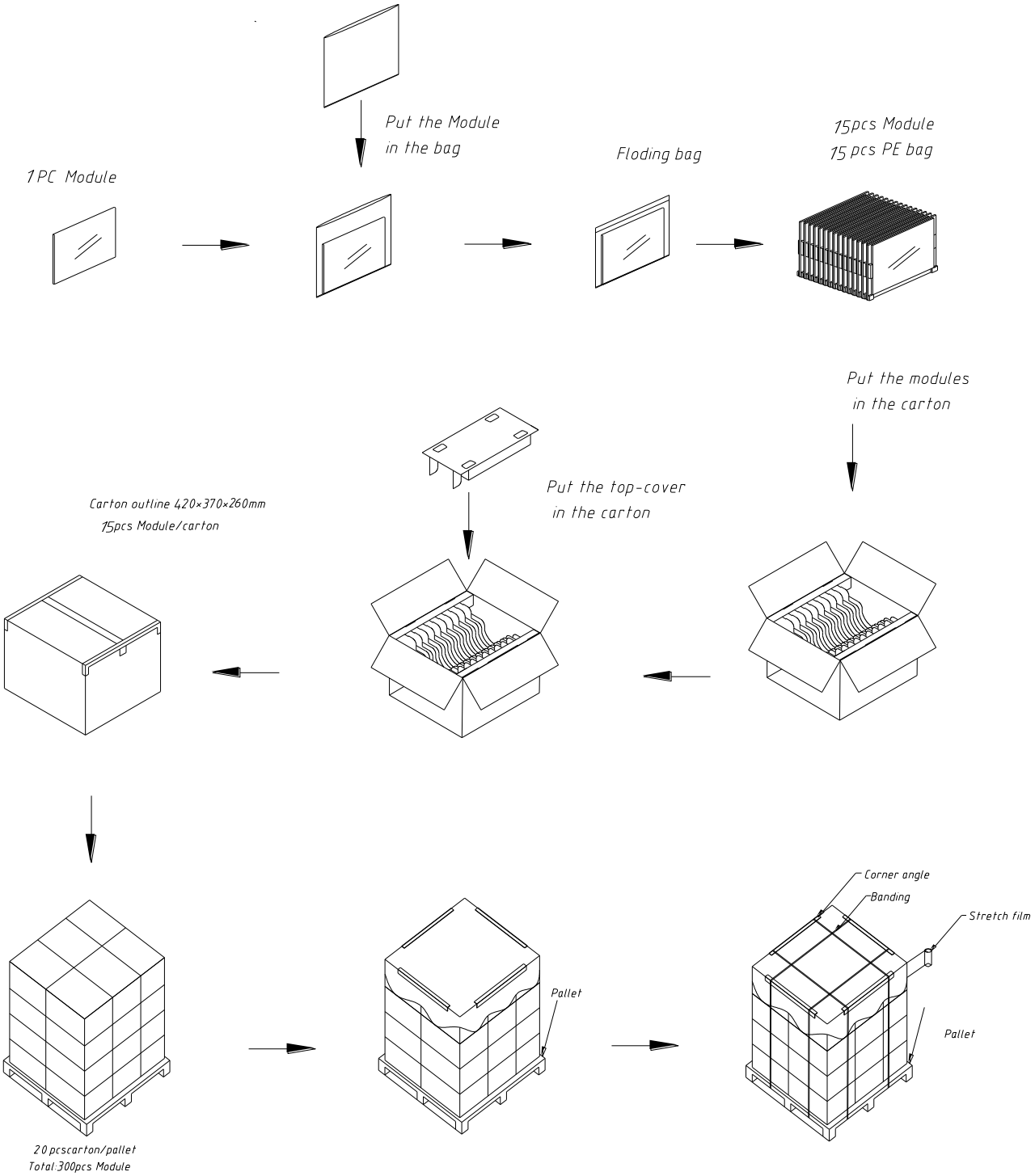


Figure 16 Packing Method