

# PRODUCT SPECIFICATION



- Tentative Specification
- Preliminary Specification
- Approval Specification

Model NO. : M315080-195-0501

<b>Customer: SMT</b>	
<b>APPROVED BY</b>	<b>SIGNATURE</b>
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## Revision History

### Record of Revisions

Rev.	Date	Sub-Model	Description of change
00	JUN, 09, 2018		N/A



## 1. General Description

### 1.1 Product Features

- **FHD Resolution (1920 x 1080)**
- **High Contrast Ratio: 4000:1**
- **Fast Response Time 6.5ms**
- **High Color Saturation: 72% NTSC**
- **Ultra Wide Viewing Angle: 178° (H)/178° (V) (CR ≥ 10)**
- **DE (Data Enable) Mode**
- **LVDS (Low Voltage Differential Signaling) Interface**

### 1.2 Overview

This is a diagonal 31.5" color active matrix LCD module with 2ch-LVDS interface. This open cell is a transmissive type display operating in the normally black mode. It supports 1920 x 1080 FHD resolution and can display up to 16.7M colors (8-bit). Each pixel is divided into Red, Green and Blue sub-pixels which are arranged in horizontal stripe. There is no backlight built-in.

This open cell dedicates for LCD TV products and provides excellent performance which includes high transmittance, ultra wide viewing angle and high color depth. CSOT open cell comply with RoHS for identification.

### 1.3 General Information

Item	Specification	Unit	Note
Active Area	698.4 (H) x 392.85 (V)	mm	
Module Size	725.2 (H) *422.7 (V) * 14.4(D)	mm	
Driving Scheme	a-Si TFT Active Matrix	-	
Number of Pixels	1920 x 1080	pixel	
Pixel Pitch(Sub Pixel)	0.12125(H) x0.36375(V)	-	
Pixel Arrangement	RGB Vertical Stripe	-	
Display Colors	16.7 M	color	8-bit
Display Mode	Transmissive Mode, Normally Black	-	
Glass thickness (Array / CF)	0.5 / 0.5	mm	
Color Chromaticity	R = 0.637, 0.334 G = 0.296, 0.611 B = 0.148, 0.060 W = 0.261, 0.274	-	Typical value measured at CSOT's module: ST3151B01-1
Contrast Ratio	4000:1 (Typ.)	-	
View Angle (CR>10)	+ 89 / - 89 (H), + 89 / - 89 (V) (Typ.)	-	
Polarizer (CF side)	Low Haze 2%, Hard Coating (3H)	-	



## 2. Absolute Maximum Ratings

### 2.1 Absolute Maximum Ratings ( $T_A = 25 \pm 2 \text{ }^\circ\text{C}$ )

The followings are maximum values which, if exceeded, may cause damage to the unit.

Item	Symbol	Value		Unit
		Min.	Max.	
Power Supply Voltage	$V_{CC}$	-0.3	13.8	V
Input Signal Voltage	$V_{IN}$	-0.3	3.6	V

### 2.2 Environment Requirement (Based on CSOT Module ST3151B01-1)

(1) Temperature and relative humidity range are shown as below.

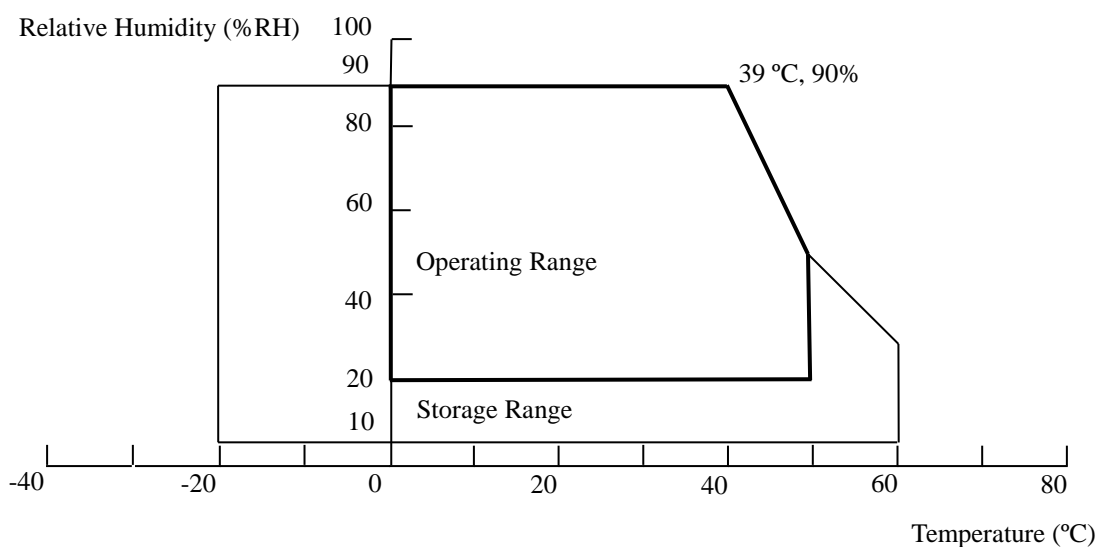


Fig. 2.1 Operating and storage environment

- (a) 90%RH maximum ( $T_A < 39 \text{ }^\circ\text{C}$ ).
- (b) Wet-bulb temperature should be 39°C maximum ( $T_A > 39 \text{ }^\circ\text{C}$ ).
- (c) No condensation.

(2) The storage temperature is between - 20 °C to 60 °C, and the operating ambient temperature is between 0 °C to 50 °C.

The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module in a temperature controlled chamber alone. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in the end product design.

(3) The rating of environment is based on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed.

Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.

### 2.3 Absolute Ratings of Environment (Open Cell)

When storing open cell as spares for a long time, please follow the precaution instructions:

- (1) Do not store the module in high temperature and high humidity for a long time. It is highly recommended to store the module with temperature from 20 °C to 30 °C in normal humidity (50 ± 10%RH) with shipping package.
- (2) The open cell should be keep within one month shelf life



### 3. Electrical Specification

#### 3.1 Open Cell Power Consumption (TA = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note	
		Min.	Typ.	Max.			
Power Supply Voltage	V <sub>CC</sub>	10.8	12.0	13.2	V	(1)	
Rush Current	I <sub>RUSH</sub>	-	-	2	A	(2)	
Power Supply Current	White Pattern	I <sub>CC</sub>	-	0.34	0.44	A	(3)
	Horizontal Stripe	I <sub>CC</sub>	-	0.52	0.67	A	
	Black Pattern	I <sub>CC</sub>	-	0.34	0.44	A	

Note:

(1) The ripple voltage should be controlled less than 10% of V<sub>CC</sub>.

(2) Measurement condition: V<sub>CC</sub> rising time = 470 μs.

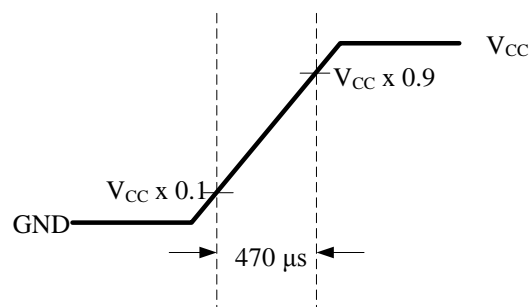


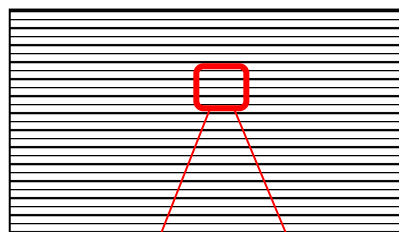
Fig. 3.1 V<sub>CC</sub> rising time condition

(3) Measurement condition: V<sub>CC</sub> = 12 V, Ta = 25 ± 2 °C, F = 75 Hz. The test patterns are shown as below.

A. White Pattern



B. Horizontal Stripe Pattern



C. Black Pattern

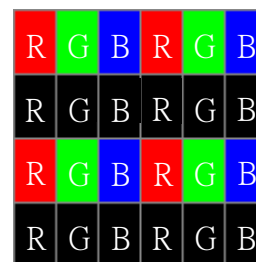


Fig. 3.2 Test patterns



### 3.2 LVDS Characteristics

Parameter	Symbol	Value			Unit	Note	
		Min.	Typ.	Max.			
LVDS Interface	Differential Input High Threshold Voltage	$V_{TH}$	+100	-	-	mV	(1)
	Differential Input Low Threshold Voltage	$V_{TL}$	-	-	-100	mV	
	Common Input Voltage	$V_{CM}$	1.0	1.2	1.4	V	
	Differential Input Voltage	$ V_{ID} $	100	-	600	mV	
	Terminating Resistor	$R_T$	87.5	100	112.5	ohm	
CMOS Interface	Input High Threshold Voltage	$V_{IH}$	2.7	-	3.3	V	
	Input Low Threshold Voltage	$V_{IL}$	0	-	0.7	V	

Note:

- (1) The product should be always operated within above ranges.
- (2) The LVDS input signal has been defined as follows:

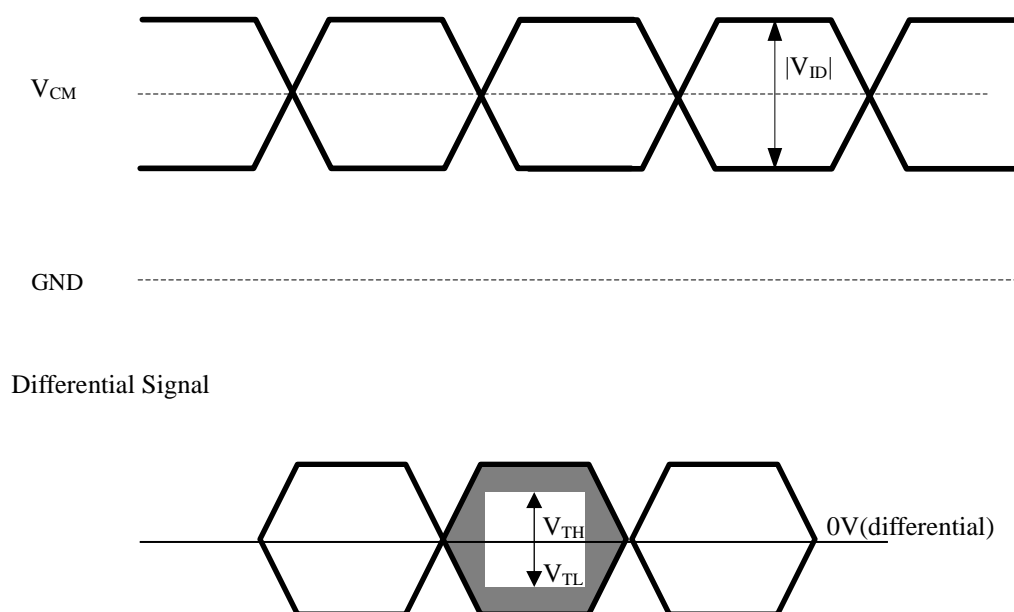


Fig. 3.3 LVDS input signal



### 3.3 Temperature Specifications

Parameter	Symbol	Specification			Unit	Recommend test pattern	Note
		Min.	Typ.	Max.			
Surface Temperature	T <sub>TCON</sub>	-	-	105	°C	Horizontal Pattern	(1)
	T <sub>Driver</sub>	-	-	115		Horizontal Pattern	(1)

Note:

- (1) Any point on the IC surface must be less than Max. specification under any condition ,If the surface temperature is out of the specification, thermal solutions should be applied to avoid be damaged;

### 3.4 Driver IC ESD Specifications

The Electro-Static Discharge tolerance of Source COF IC is +-2KV tested by ESD Gun. Especially if the LCD module is designed with the Plastic Bezel, we suggest ESD protection solutions should be applied to avoid be damaged, as shown in Fig.3.4

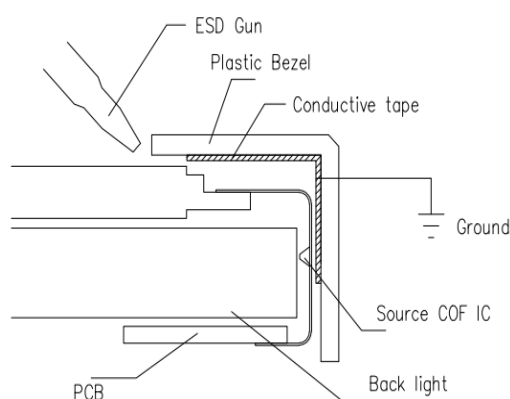


Fig. 3.4 Source COF IC ESD protection



## 4. Input Terminal Pin Assignment

### 4.1 Interface Pin Assignment

CN1: F05035-51P-K (昶通) or equivalent (see Note (1))

Pin No.	Symbol	Description	Note
1	WP	Write Protect (High: Write Enable, Low or Open: Write Disable )	(2)
2	SCL	I2C Serial Clock (for adjust VCOM)	(2)
3	SDA	I2C Serial Data (for adjust VCOM)	(2)
4	NC	No Connection	(3)
5	NC	No Connection	(3)
6	NC	No Connection	(3)
7	LVDS_SEL	LVDS Data Format Selection	(4)
8	NC	No Connection	(3)
9	NC	No Connection	(3)
10	NC	No Connection	(3)
11	GND	Ground	
12	RO[0]N	Odd LVDS Signal -	
13	RO[0]P	Odd LVDS Signal +	
14	RO[1]N	Odd LVDS Signal -	
15	RO[1]P	Odd LVDS Signal +	
16	RO[2]N	Odd LVDS Signal -	
17	RO[2]P	Odd LVDS Signal +	
18	GND	Ground	
19	ROCLK-	Odd LVDS Clock -	
20	ROCLK+	Odd LVDS Clock +	
21	GND	Ground	
22	RO[3]N	Odd LVDS Signal -	
23	RO[3]P	Odd LVDS Signal +	
24	NC	No Connection	(3)
25	NC	No Connection	(3)
26	NC	No Connection	(3)
27	NC	No Connection	(3)
28	RE[0]N	Even LVDS Signal -	
29	RE[0]P	Even LVDS Signal +	
30	RE[1]N	Even LVDS Signal -	
31	RE[1]P	Even LVDS Signal +	
32	RE[2]N	Even LVDS Signal -	
33	RE[2]P	Even LVDS Signal +	



34	GND	Ground	
35	RECLK-	Even LVDS Clock -	
36	RECLK+	Even LVDS Clock +	
37	GND	Ground	
38	RE[3]N	Even LVDS Signal -	
39	RE[3]P	Even LVDS Signal +	
40	NC	No Connection	(3)
41	NC	No Connection	(3)
42	NC	No Connection	(3)
43	NC	No Connection	(3)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	NC	No Connection	
48	12V	DC power supply	
49	12V	DC power supply	
50	12V	DC power supply	
51	12V	DC power supply	

Note:

(1)The direction of pin assignment is shown as below:

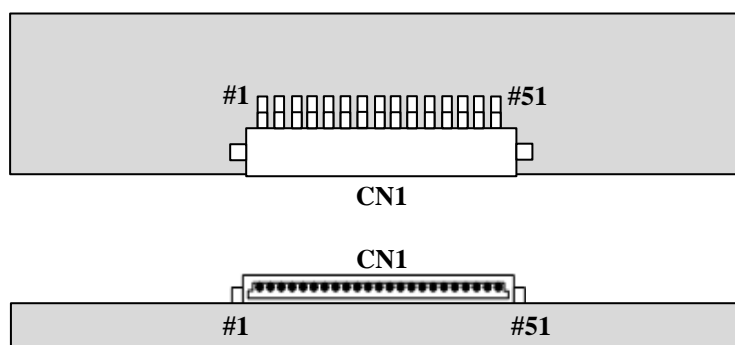


Fig. 4.1 LVDS connector direction sketch map



(2) a. Please let it open (Do not line out from PCBA connector) if it do not used.(for example : TV set )

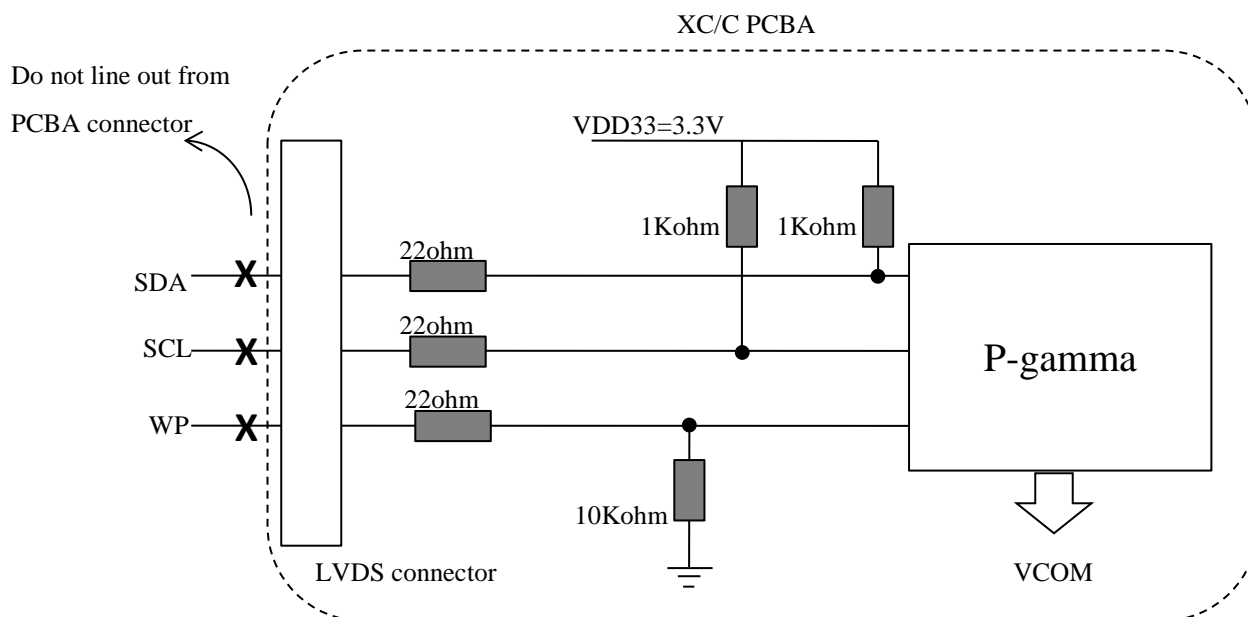


Fig. 4.2 WP/SDA/SCL PCBA set

b. For the VCOM (Flicker) regulation and control, SDA and SCL must pull high in the flicker set, and the flicker set's VDD must ready before the input power (VCC12V)

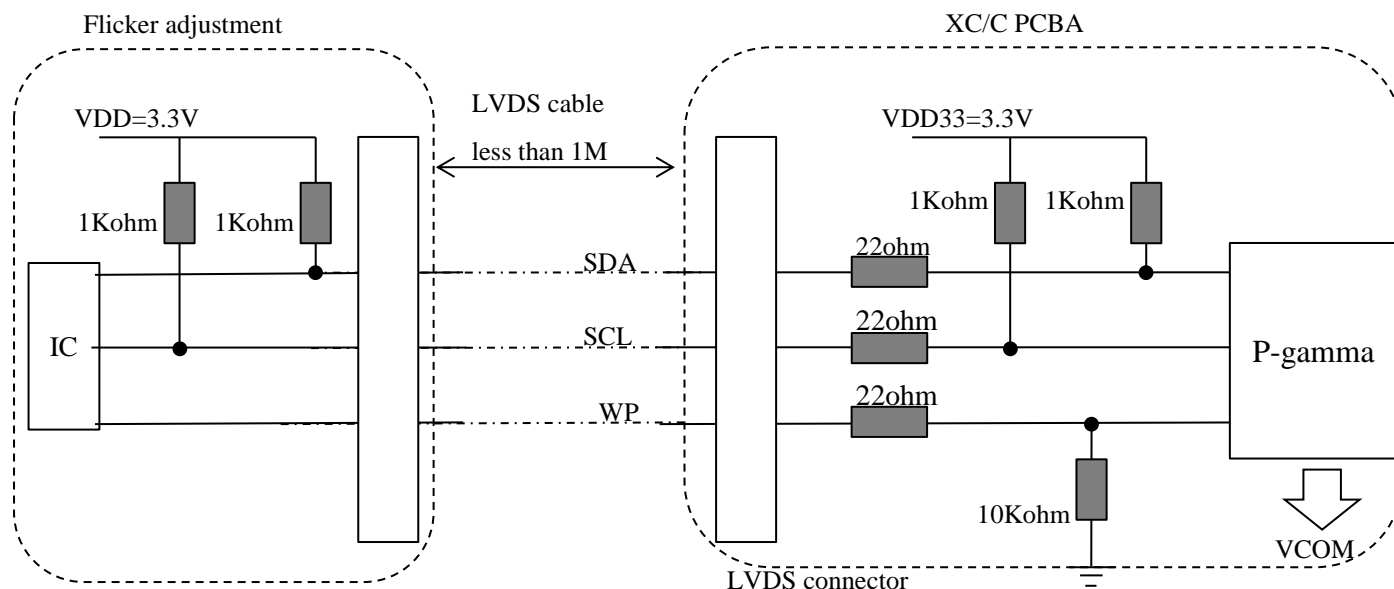


Fig. 4.3 WP/SDA/SCL flicker set

(3) For CSOT internal only, please let it open.



(4) High: connect to + 3.3 V → JEIDA format; Low: connect to GND or Open → VESA format.

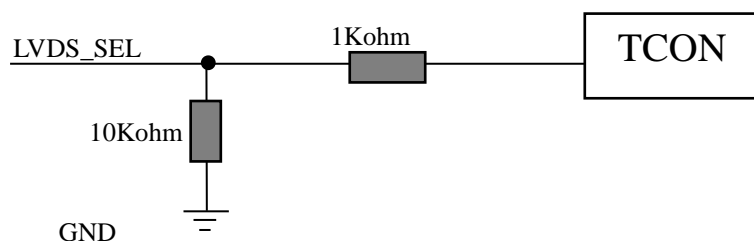


Fig. 4.4 LVDS\_SEL PCBA set

## 4.2 Block Diagram of Interface

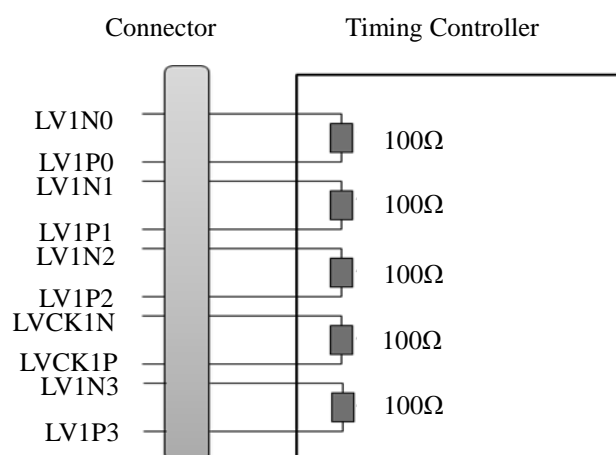


Fig. 4.5 Block diagram of interface

Attention:

- (1) This open cell uses a 100 ohms ( $\Omega$ ) resistor between positive and negative lines of each receiver input.
- (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line respectively

## 4.3 LVDS Interface

### 4.3.1 VESA Format (SELLVDS = L or Open)

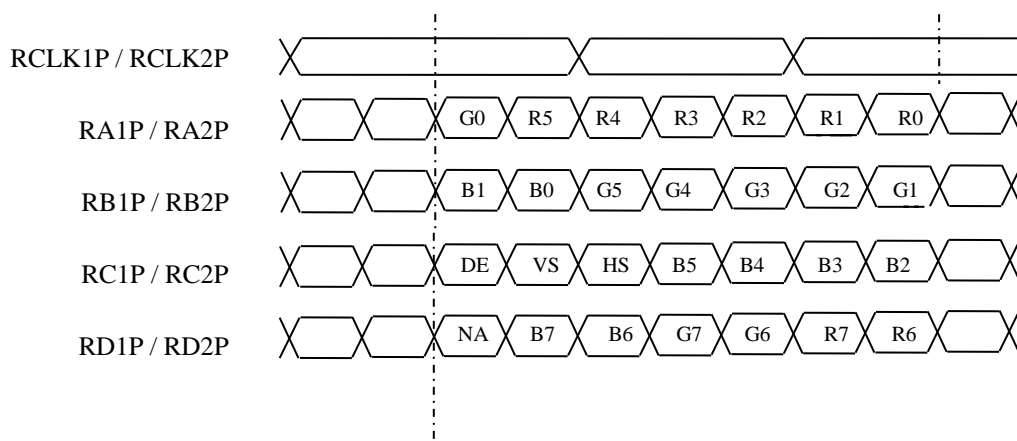


Fig. 4.6 VESA format

#### 4.3.2 JEIDA Format (SELLVDS = H)

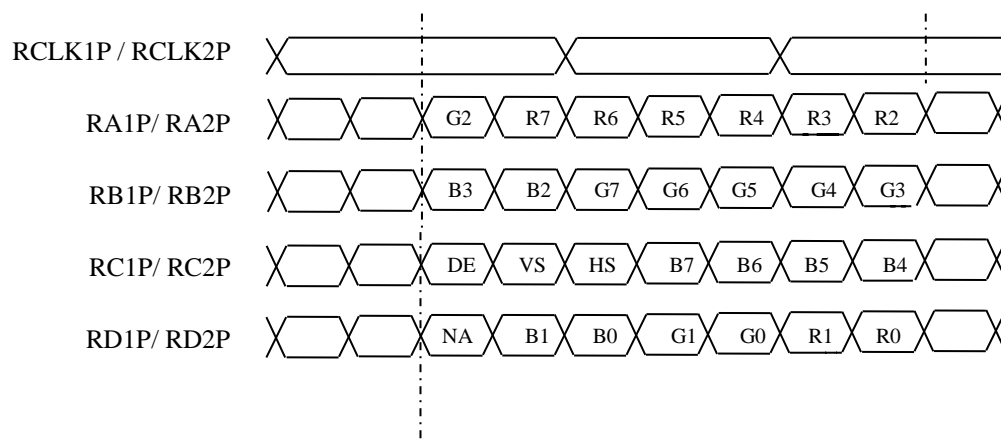


Fig. 4.7 JEIDA format

### 4.4 V-com Adjustment

(a) Flicker should be adjusted by optimizing the Vcom value in customer LCM line through the I2C interface. (Master & Slave = I2C communication)

Pin. NO.	Symbol	Function	Remark
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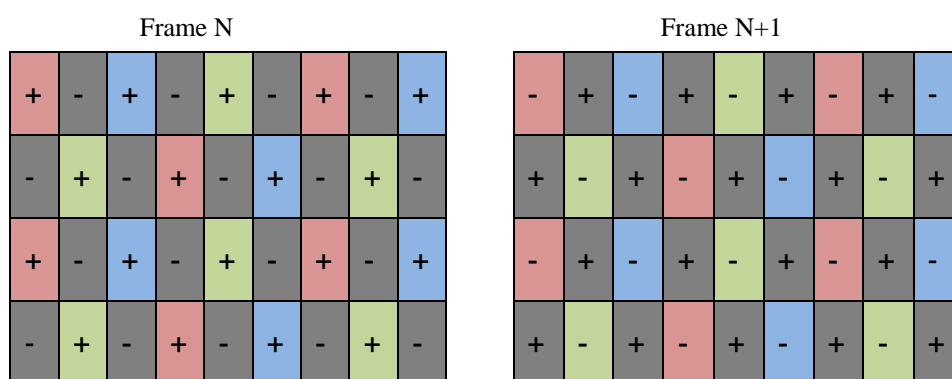
1	WP	EN	Default:0V Vcom tuning:3.3V (Shouldn't be communicated with I2C device as output level "5V")
2	SCL_I	I2C Interface	I2C Interface
3	SDA_I	I2C Interface	

(b) Flicker should be tuned by correct method according to gamma IC type of each model.

Type	Flicker data saving position	Slave Address							
Genie Type	Gamma IC memory	B7	B6	B5	B4	B3	B2	B1	B0
		1	1	1	0	1	0	0	R/W-

(c) Flicker Should be adjusted by the Dot on/off pattern

Dot on/off pattern



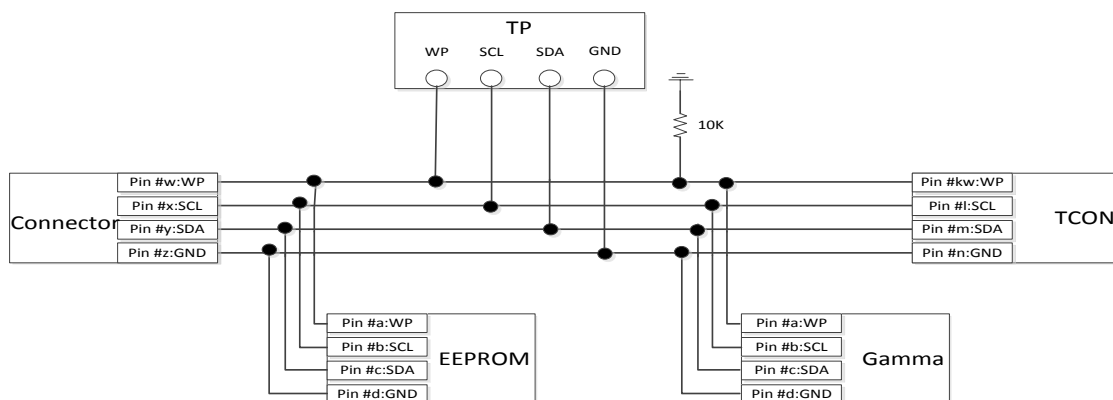


Fig 4.8 Flicker adjust circuit block diagram



## 5. Interface Timing

### 5.1 Timing Table (DE Only Mode)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	Fclkin (=1/T <sub>CLK</sub> )	65	74.25	96	MHz	(1) (2)
	Input cycle to cycle jitter	Trcl	—	—	200	ps	(3)
	Spread spectrum modulation range	Fclkin_mod	Fclkin-2%	—	Fclkin+2%	MHz	(4)
	Spread spectrum modulation frequency	F <sub>SSM</sub>	60	—	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	T <sub>RSM</sub>	-400	—	400	ps	(5)
Vertical Active Display Term	Frame Rate	F	48	60	75	Hz	
	Total	T <sub>V</sub>	1092	1125	1380	T <sub>H</sub>	T <sub>V</sub> = T <sub>VD</sub> + T <sub>VB</sub>
	Display	T <sub>VD</sub>	1080			T <sub>H</sub>	
	Blank	T <sub>VB</sub>	12	45	300	T <sub>H</sub>	
Horizontal Active Display Term	Total	T <sub>H</sub>	1046	1100	1174	T <sub>CLK</sub>	T <sub>H</sub> = T <sub>HD</sub> + T <sub>HB</sub>
	Display	T <sub>HD</sub>	960			T <sub>CLK</sub>	
	Blank	T <sub>HB</sub>	86	140	214	T <sub>CLK</sub>	

Note:

(1) The TFT LCD open cell is operated in DE only mode, H sync and V sync input signal have no effect on normal operation.

(2) Please make sure the range of pixel clock follows the following equations:

$$F_{clkin(max)} \geq F_{max} \times T_v \times T_h \quad F_{min} \times T_v \times T_h \geq F_{clkin(min)}$$

Main frequency Max is 96MHz without spread spectrum

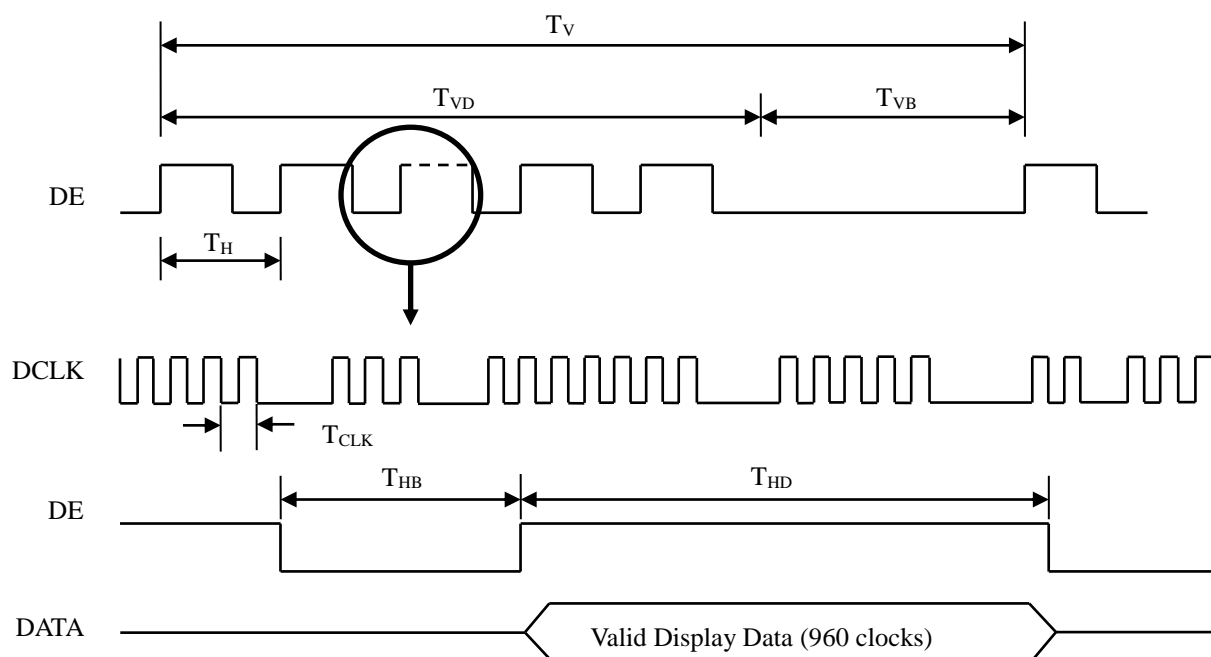


Fig. 5.1 Interface signal timing diagram

(3)The input clock cycle-to-cycle is defined as below figures.

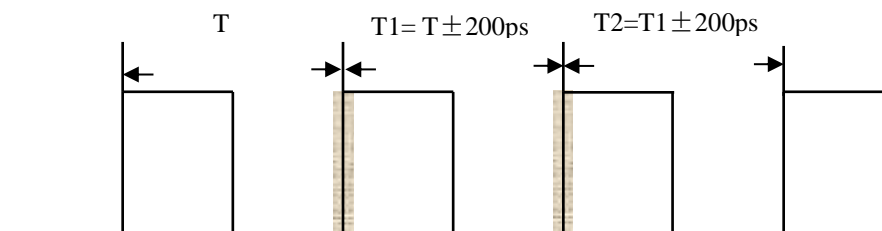


Fig. 5.2 Jitter



(4) The SSCG (Spread Spectrum Clock Generator) is defined as the following figure.

The LVDS SSM's suggestion is off by default, SOC board must test all validation if SOC board open the LVDS SSM.

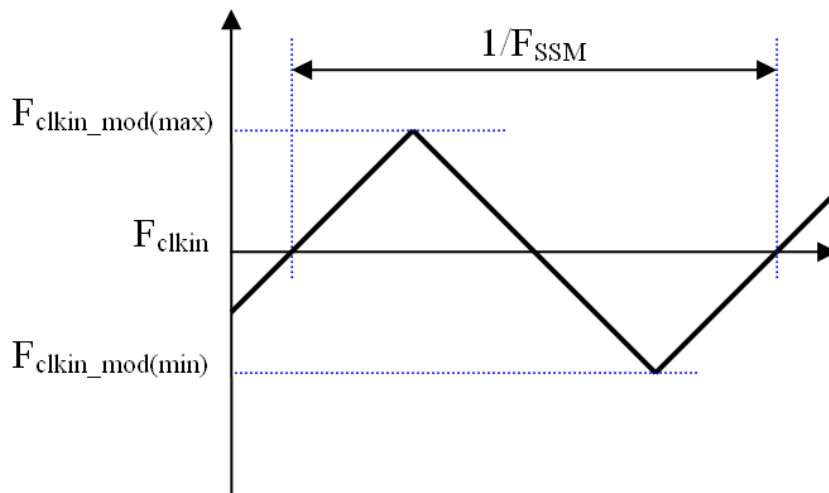


Fig. 5.3 SSCG

(5) The LVDS timing diagram and setup/hold time is defined and showed as the following figure.

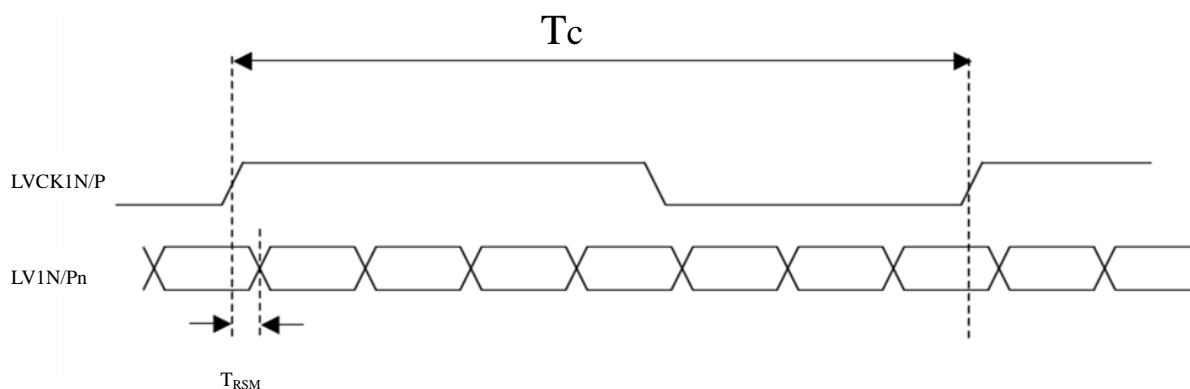


Fig.5.4 LVDS receive interface timing diagram



## 5.2 Power On/Off Sequence

To prevent a latch-up or DC operation of the Open cell, the power on/off sequence should be as the diagram below.

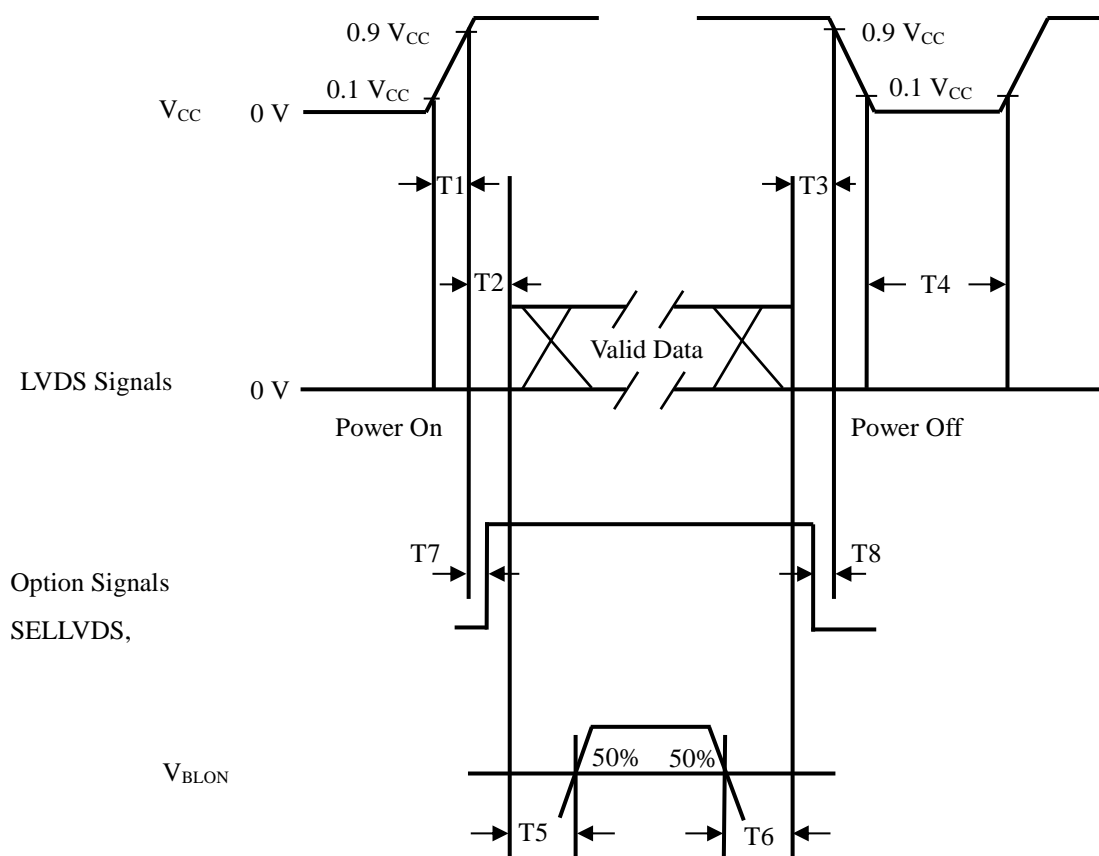


Fig.5.5 Power on/off sequence

Parameter	Values			Unit Min.
	Min.	Typ.	Max.	
T1	0.5	-	10.0	ms
T2	0.0	-	50	ms
T3	0.0	-	50	ms
T4	1000.0	-	-	ms
T5	500.0	-	-	ms
T6	100.0	-	-	ms
T7	-	-	T2	ms
T8	-	-	T3	ms



**Attention:**

- (1) The supply voltage of the external system for the open cell input should follow the definition of VCC.
- (2) When the customer's backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.
- (3) In case that VCC is in off level, please keep the level of input signals on the low or high impedance. If  $T2 < 0$ , that may cause electrical overstress.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.

### 5.3 Backlight Unit

The following shows the block diagram of the 31.5 inch Backlight Unit. And it includes 80 pcs LED in the LED light bar. (10 strings and 8pcs LED of one string).

#### LED LIGHTBAR UNIT CHARACTERISTICS

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lightbar input Voltage	V	50.4	57.6	61.2	V <sub>RMS</sub>	
Lightbar input current	I <sub>L</sub>		750		mA	
Power consume	W		43.2		W	
Lightbar Life Time	L <sub>BL</sub>	20000		-	Hrs	

## 6. Optical Characteristics

### 6.1 Measurement Conditions

The table below is the test condition of optical measurement.

Item	Symbol	Value	Unit
Ambient Temperature	$T_A$	$25 \pm 2$	$^{\circ}\text{C}$
Ambient Humidity	$H_A$	$50 \pm 10$	% RH
Supply Voltage	$V_{CC}$	12	V
Driving Signal	Refer to the typical value in Chapter 3: Electrical Specification		
Vertical Refresh Rate	$F_R$	60	Hz

To avoid abrupt temperature change during optical measurement, it's suggested to warm up the LCD module more than 45 minutes after lighting the backlight and in the windless environment.

To measure the LCD cell, it is suggested to set up the standard measurement system as Fig. 6.1. The measuring area  $S$  should contain at least 500 pixels of the LCD cell as illustrated in Fig.6.2 ( $A$  means the area allocated to one pixel). In this model, for example, the minimum measuring distance  $Z$  is 370 mm when  $\theta$  is 2 degree. Hence, 500 mm is the typical measuring distance. This measuring condition is referred to 301-2H of VESA FPDM 2.0 about viewing distance, angle, and angular field of view definition.

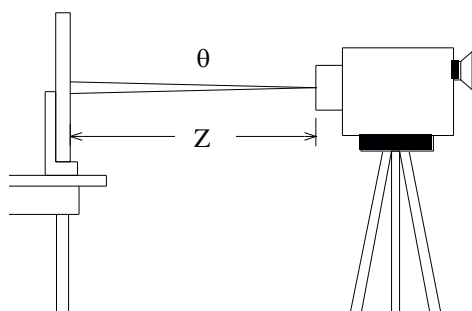


Fig. 6.1 The standard set-up system of measurement

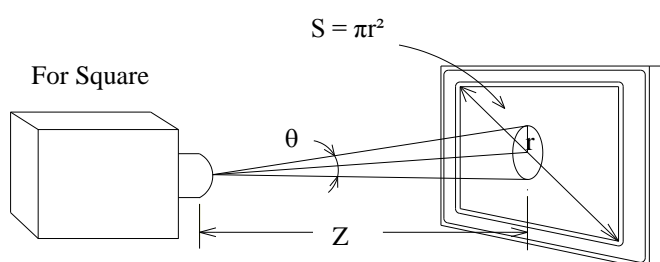


Fig. 6.2 The area  $S$  contains at least 500 pixels to be measured

$$N = \frac{S}{A} \geq 500\text{pixels}$$

$N$  means the actual number of the pixels in the area  $S$ .



## 6.2 Optical Specifications

The table below of optical characteristics is measured by MINOLTA CS2000, MINOLTA CA310, ELDIM OPTI Scope-SA and ELDIM EZ contrast in dark room. (The optical data in the form is measured by matching the backlight of ST3151B01-1.)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Static Contrast Ratio		CR	$\theta_H = 0^\circ, \theta_V = 0^\circ$	3200	4000	-	-	(1) (2)
Response Time		$T_L$		-	6.5	-	ms	(3)
Center Transmittance		T%		-	4.7	-	%	(2) (4)
Color Chromaticity (CIE1931)	Red	$R_X$		Typ. - 0.03	Typ. + 0.03	0.637	-	(2) (5)
		$R_Y$				0.334	-	
	Green	$G_X$				0.296	-	
		$G_Y$				0.611	-	
	Blue	$B_X$				0.148	-	
		$B_Y$				0.060	-	
	White	$W_X$				0.261	-	
		$W_Y$	0.274			-		
Color Gamut		CG	-	72	-	% NTSC		
Viewing Angle	Horizontal	$\theta_{H+}$	$CR \geq 10$	80	89	-	Deg.	(6)
		$\theta_H$						
	Vertical	$\theta_{V+}$						
		$\theta_V$						
$L_w$	White Luminance (Center of screen)		700	1000	-	[cd/m <sup>2</sup> ]		

Note:

(1) Definition of static contrast ratio (CR):

It's necessary to switch off all the dynamic and dimming function when measuring the static contrast ratio.

$$\text{Static Contrast Ratio (CR)} = \frac{\text{CR-W}}{\text{CR-D}}$$

CR-W is the luminance measured by LMD (light-measuring device) at the center point of the LCD module with full-screen displaying white. The standard setup of measurement is illustrated in Fig. 6.3; CR-D is the luminance measured by LMD at the center point of the LCD module with full-screen displaying black. The LMD in this item is CS2000.

(2) The LMD in the item could be a spectroradiometer such as (KONICA MINOLTA) CS2000, CS1000(TOPCON), SR-UL2 or the same level spectroradiometer. Other display color analyzer (KONICA MINOLTA) CA210, CA310 or (TOPCON) BM-7 could be involved after being calibrated with a spectroradiometer on each stage of a product.

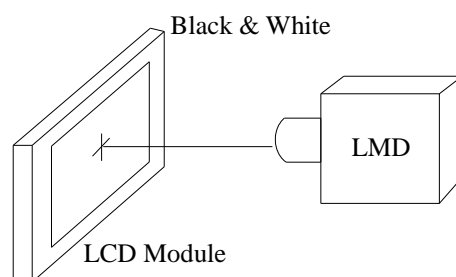


Fig. 6.3 The standard setup of CR measurement

(3) Response time  $T_L$  is defined as the average transition time in the response time matrix. The table below is the response time matrix in which each element  $t_{X \text{ to } Y}$  is the transition time from luminance ratio  $X$  to  $Y$ .  $X$  and  $Y$  are two different luminance ratios among 0%, 25%, 50%, 75%, and 100% luminance. The transition time  $t_{X \text{ to } Y}$  is defined as the time taken from 10% to 90% of the luminance difference between  $X$  and  $Y$  ( $X < Y$ ) as illustrated in Fig.6.4. When  $X > Y$ , the definition of  $t_{X \text{ to } Y}$  is the time taken from 90% to 10% of the luminance difference between  $X$  and  $Y$ . The response time is optimized on refresh rate  $F_r = 60\text{Hz}$ .

Measured Transition Time		Luminance Ratio of Previous Frame				
		0%	25%	50%	75%	100%
Luminance Ratio of Current Frame	0%		$t_{25\% \text{ to } 0\%}$	$t_{50\% \text{ to } 0\%}$	$t_{75\% \text{ to } 0\%}$	$t_{100\% \text{ to } 0\%}$
	25%	$t_{0\% \text{ to } 25\%}$		$t_{50\% \text{ to } 25\%}$	$t_{75\% \text{ to } 25\%}$	$t_{100\% \text{ to } 25\%}$
	50%	$t_{0\% \text{ to } 50\%}$	$t_{25\% \text{ to } 50\%}$		$t_{75\% \text{ to } 50\%}$	$t_{100\% \text{ to } 50\%}$
	75%	$t_{0\% \text{ to } 75\%}$	$t_{25\% \text{ to } 75\%}$	$t_{50\% \text{ to } 75\%}$		$t_{100\% \text{ to } 75\%}$
	100%	$t_{0\% \text{ to } 100\%}$	$t_{25\% \text{ to } 100\%}$	$t_{50\% \text{ to } 100\%}$	$t_{75\% \text{ to } 100\%}$	

$t_{X \text{ to } Y}$  means the transition time from luminance ratio  $X$  to  $Y$ .

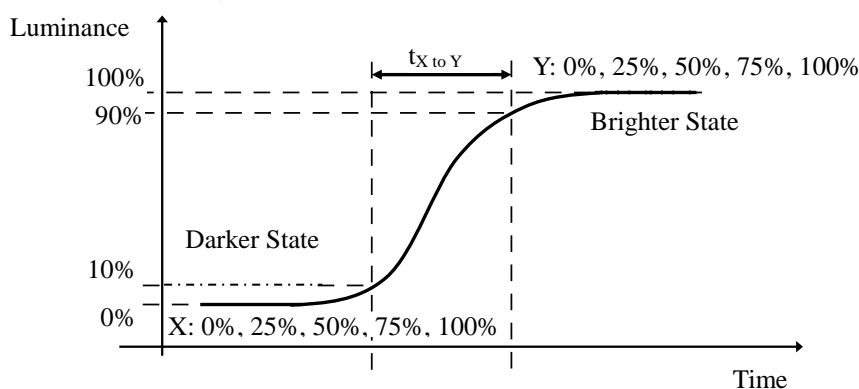


Fig. 6.4 The definition of  $t_{X \text{ to } Y}$

All the transition time is measured at the center point of the LCD module by ELDIM OPTI Scope-SA.

(4) Definition of center Transmittance (T%):

The transmittance is measured with full white pattern (Gray 255)

$$\text{Center Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of Backlight}}$$

(5) Definition of color chromaticity:

Each chromaticity coordinates (x, y) are measured in CIE1931 color space when full-screen displaying primary color R, G, B and white. The color gamut is defined as the fraction in percent of the area of the triangle bounded by R, G, B coordinates and the area is defined by NTSC 1953 color standard in the CIE color space. Chromaticity coordinates are measured by CS2000 and the standard setup of measurement is shown in Fig. 6.5.

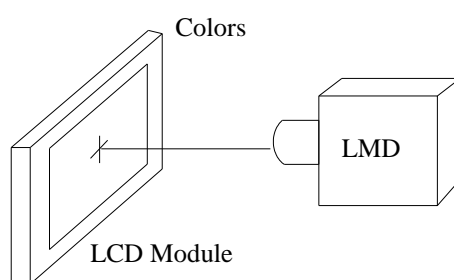


Fig. 6.5 The standard setup of color chromaticity measurement

(6) Definition of viewing angle coordinate system ( $\theta_H$ ,  $\theta_V$ ):

The contrast ratio is measured at the center point of the LCD module. The viewing angles are defined at the angle that the contrast ratio is larger than 10 at four directions relative to the perpendicular direction of the LCD module (two vertical angles: up  $\theta_{V+}$  and down  $\theta_{V-}$ ; and two horizontal angles: right  $\theta_{H+}$  and left  $\theta_{H-}$ ) as illustrated in Fig. 6.6. The contrast ratio is measured by ELDIM EZ Contrast.

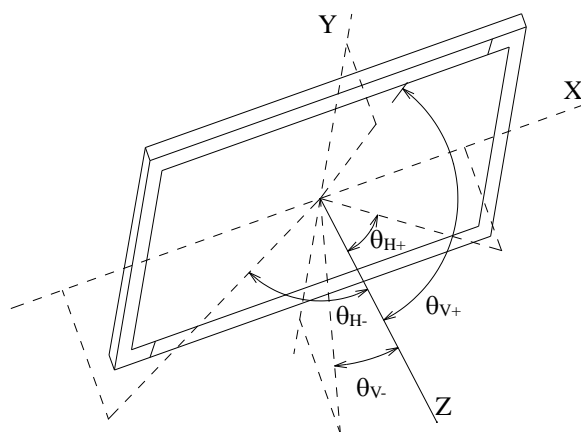


Fig. 6.6 Viewing angle coordination system



## 7. Mechanical Characteristics

