

CUSTOMER APPROVE

SPECIFICATION
FOR
DOUBLE LIN TFT-LCD MODULE

Edition : Preliminary spec 1.0

Date of issue : 2022-05-03

Product No. : HV320FHB-N02

APPROVED	CHECKED	PREPARED
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Revision History

Date	Rev.	Page	Old Description	New Description	Remark
2022-05-03	1.0	All	The specification was first issued		

CONTENTS

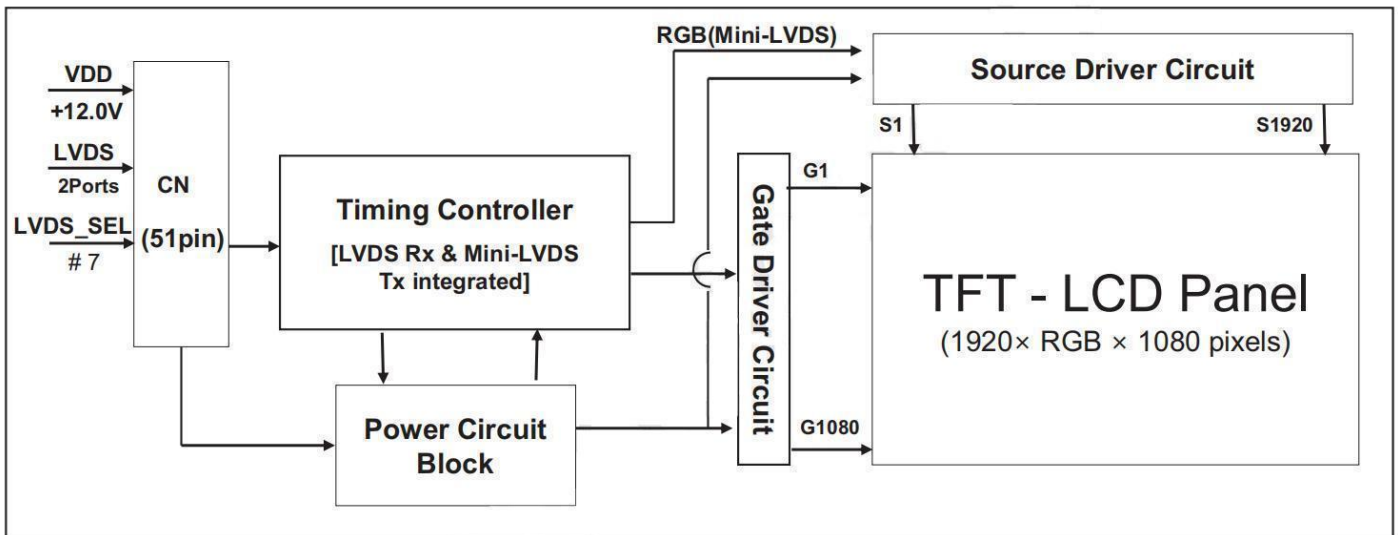
目录

SPECIFICATION -----	1
DOUBLE LIN TFT-LCD MODULE -----	1
Revision History -----	2
CONTENTS -----	3
1.General Description -----	4
1.1 Introduction -----	4
1.2.Features -----	4
1.3 Application -----	4
1.4 General Specification -----	5
2. Absolute Maximum Ratings -----	6
3. Electrical Specifications -----	7
3.1 Open Cell Power Consumption (TA=25 ±2°C) -----	7
4. Interface connection -----	8
4.1 Module Input Signal & Power -----	8
5. Signal Timing Specification -----	9
5.1 Timing Parameters(DE only moed) -----	9
5.2 Signal Timing Waveform -----	10
5.3 Input Signals,Basic Display Colors adn Gray Scale of Colors -----	11
5.4 Power Sequence -----	12
6. Mini-LVDS Signal Specifications -----	12
7. Optical Specifications -----	13
8. Mechanical characteristics -----	15
8.1 Dimensional Requirements -----	15
8.2 Semi-Glare and Polarizer Hardness -----	15
9. Reliability Test Condition -----	15
10. Bcaklight Unit -----	16
10.1 LED Pin Assignment -----	16
10.2 Recommednded Operating Condition -----	16
11. Appendix -----	17
12. Shipping Label -----	18
13. Precaution -----	19
13.1 Assembly and handling precautions -----	19
13.2 Safety precautions -----	20

1.General Description

1.1 Introduction

HV320FHB-N02 is a color active matrix TFT LCD open cell using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This open cell has a 31.51 inch diagonally measured active area with FHD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this open cell can display 16.7M colors. The TFT-LCD panel used for this open cell is adapted for a low reflection and higher color type.



1.2.Features

- LVDS interface with 2 pixel / clock
- High-speed response
- Low color shift image quality
- 8-bit color depth, display 16.7M colors
- High luminance and contrast ratio, low reflection and wide viewing angle
- DE (Data Enable) only mode
- ADSDS technology is applied for high display quality
- RoHS compliant

1.3 Application

- Home Alone Multimedia TFT-LCD TV
- Display Terminals for Control System
- High Definition TV(FHD TV)
- AV application Products

1.4 General Specification

<Table 1. General Specifications>

Items	Unit	Specifications
Screen Diagonal	[mm]	32
Active Area	[mm]	698.4(H) × 392.85 (V)
Pixels H x V	-	1920(H) × 1080(V)
Pixels Pitch	[mm]	121.25(H) × RGB× 363.75(V)
Pixels Arrangement	-	Pixels RGB Vertical stripe
White Luminance(Center)	[cd/m ²]	300 (Typ.)
Contrast Ratio	-	1200 (Typ.)
Response Time	[msec]	8ms (Typ.on/off)
Viewing Angle	[degree]	89/89/89/89
Outline Dimension	[mm]	725.2(H) x 422.7V) x 14.9(D) (Typ.)
Electrical Interface	-	Dual Channel LVDS
Support Color		16.7M colors
Surface Treatment		Haze:25% 3H
Temperature Range Operating Storage(Shipping)	[oC] [oC]	0 to +50°C -20 to+60°C

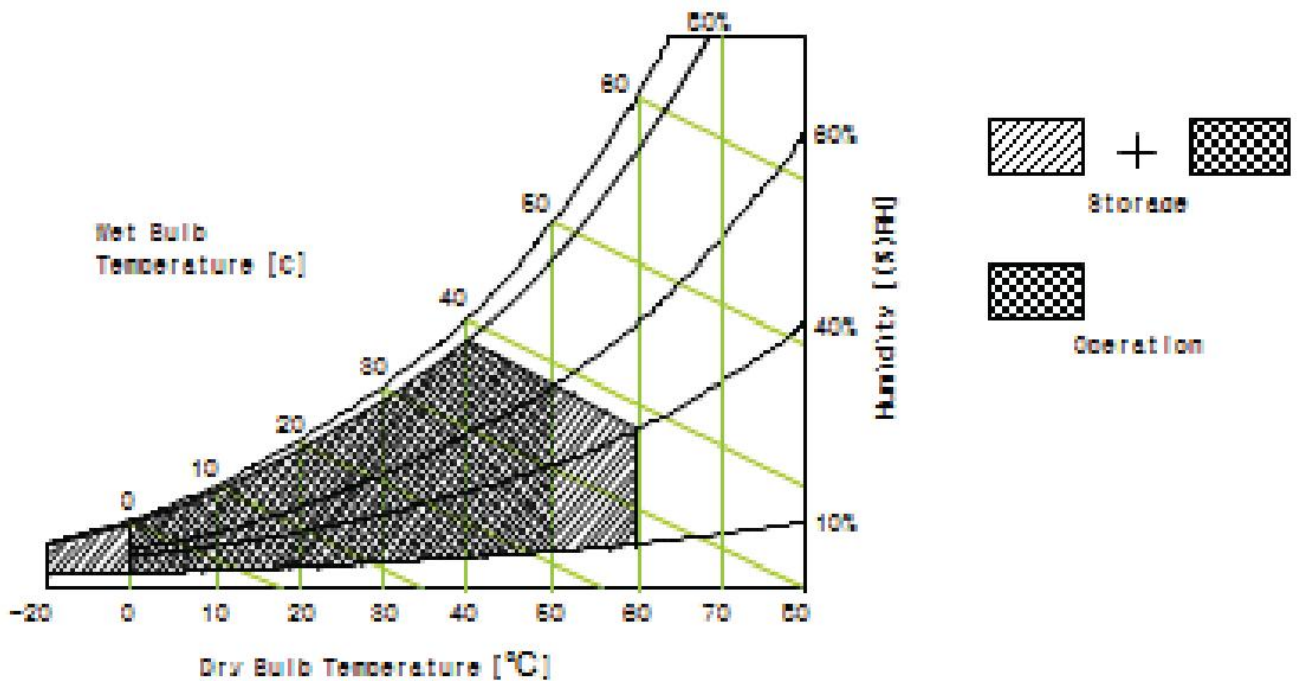
2. Absolute Maximum Ratings

The followings are maximum values which ,if exceed,may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2

<Table 2. Absolute Maximum Ratings>

Parameter	Symbol	Min	Max	Unit	Remarks
Power Supply Voltage	VDD	VSS-0.3	14	V	Ta=25°C
Operating Temperature	TOP	0	+50	°C	Note 1
	TSUR	0	+60	°C	
Storage Temperature	TST	-20	+60	°C	
Operating Ambient Humidity	Hop	10	80	%RH	
Storage Humidity	Hst	10	80	%RH	

Note 1-1 :Temperature and relative humidity range are shown as the below .
Wet bulb temperature should 39°C max .and no condensation of water.



3. Electrical Specifications

3.1 Open Cell Power Consumption (TA=25 ±2 °C)

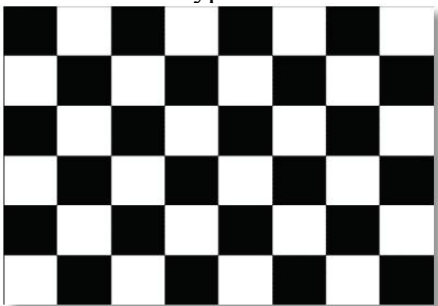
Parameter		Symbol	Values			Unit	Remarks
			Min.	Typ.	Max.		
Power Supply Input Voltage		VDD	10.8	12	14	Vdc	
Power Supply Ripple Voltage		VRP	-		300	mV	
Power Supply Current		IDD	-	333	630	mA	Note 1
Power Consumption		PDD	-	4.0	7.6	Watt	
Rush current		IRUSH	-	-	3.3	A	Note 2
LVDS Interface	LVDS Swing Voltage	VID	± 100	-	± 600	mV	Note 3
	Common Input Voltage	VLVC	1.0	1.2	1.4	V	
CMOS Interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.6	V	

Notes:1. The supply voltage is measured and specified at the interface connector of LCM.

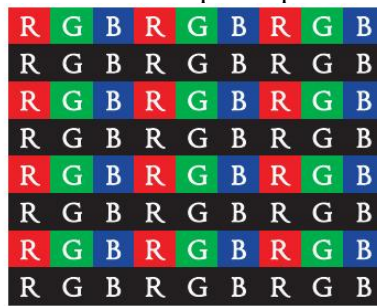
The current draw and power consumption specified is for VDD=12.0V,Frame rate=60Hz Clock frequency =75.4MHz.

Test Pattern of power supply current

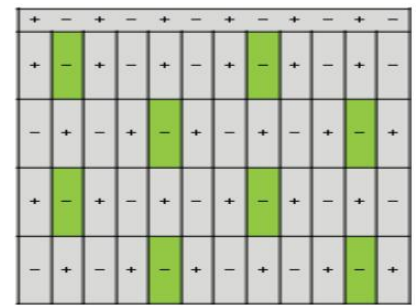
a. Typ: Color Test



b. Max: Skip Sud-pixel



c. Flicker Pattern



Note 2: The duration of rush current is about 2ms and rising time of Power Input is 1ms(min)

Note 3: The LVDS test point is at each terminal resistor

4. Interface connection

4.1 Module Input Signal & Power

- Connector : IS050-C51B-C39-S (UJU) / FI-RE51S-HF-R1500 (JAE) or Equivalent.

< Table 4. Open Cell Input Connector Pin Configuration >

Pin No	Symbol	Description	Pin No	Symbol	Description
1	NC	No Connection	21	GND	Ground
2	SDA	I2C Data	22	CH1[3]-	First pixel negative LVDS differential data input. Pair3
3	SCL	I2C Clock	23	CH1[3]+	First pixel positive LVDS differential data input. Pair3
4	NC	Not Connected	24	NC	Not Connected
5	NC	Not Connected	25	NC	Not Connected
6	NC	Not Connected	26	NC	Not Connected
7	SELLVDS	High: JEIDA Low or Open: VESA	27	NC	Not Connected
8	NC	Not Connected	28	CH2[0]-	Second pixel negative LVDS differential data input. Pair0
9	NC	Not Connected	29	CH2[0]+	Second pixel positive LVDS differential data input. Pair0
10	NC	Not Connected	30	CH2[1]-	Second pixel negative LVDS differential data input. Pair1
11	GND	Ground	31	CH2[1]+	Second pixel positive LVDS differential data input. Pair1
12	CH1[0]-	First pixel negative LVDS differential data input. Pair0	32	CH2[2]-	Second pixel negative LVDS differential data input. Pair2
13	CH1[0]+	First pixel positive LVDS differential data input. Pair0	33	CH2[2]+	Second pixel positive LVDS differential data input. Pair2
14	CH1[1]-	First pixel negative LVDS differential data input. Pair1	34	GND	Ground
15	CH1[1]+	First pixel positive LVDS differential data input. Pair1	35	CH2CLK-	Second pixel negative LVDS clock
16	CH1[2]-	First pixel negative LVDS differential data input. Pair2	36	CH2CLK+	Second pixel positive LVDS clock
17	CH1[2]+	First pixel positive LVDS differential data input. Pair2	37	GND	Ground
18	GND	Ground	38	CH2[3]-	Second pixel negative LVDS differential data input. Pair3
19	CH1CLK-	First pixel negative LVDS clock	39	CH2[3]+	Second pixel positive LVDS differential data input. Pair3
20	CH1CLK+	First pixel positive LVDS clock			
40	NC	Not Connected	46	GND	Ground
41	NC	Not Connected	47	NC	Not Connected
42	NC or GND	Not Connected	48	VCC	Input Voltage +12V
43	NC or GND	Not Connected	49	VCC	Input Voltage +12V
44	NC or GND	Ground	50	VCC	Input Voltage +12V
45	GND	Ground	51	VCC	Input Voltage +12V

Notes: 1. NC (Not Connected) : This pins are only used for BOE internal operations.
 Input Level of LVDS signal is based on the IEA 664 Standard.
 LVDS_SEL: This pin is used for selecting LVDS signal data format.
 If this Pin: High(3.3V)→JEIDA LVDS format
 Otherwise : Low (GND) or Open (NC) → Normal NS LVDS format

Rear view of LCM

BIST Pattern



5. Signal Timing Specification

5.1 Timing Parameters(DE only moed)

<Table 5. Timing Table>

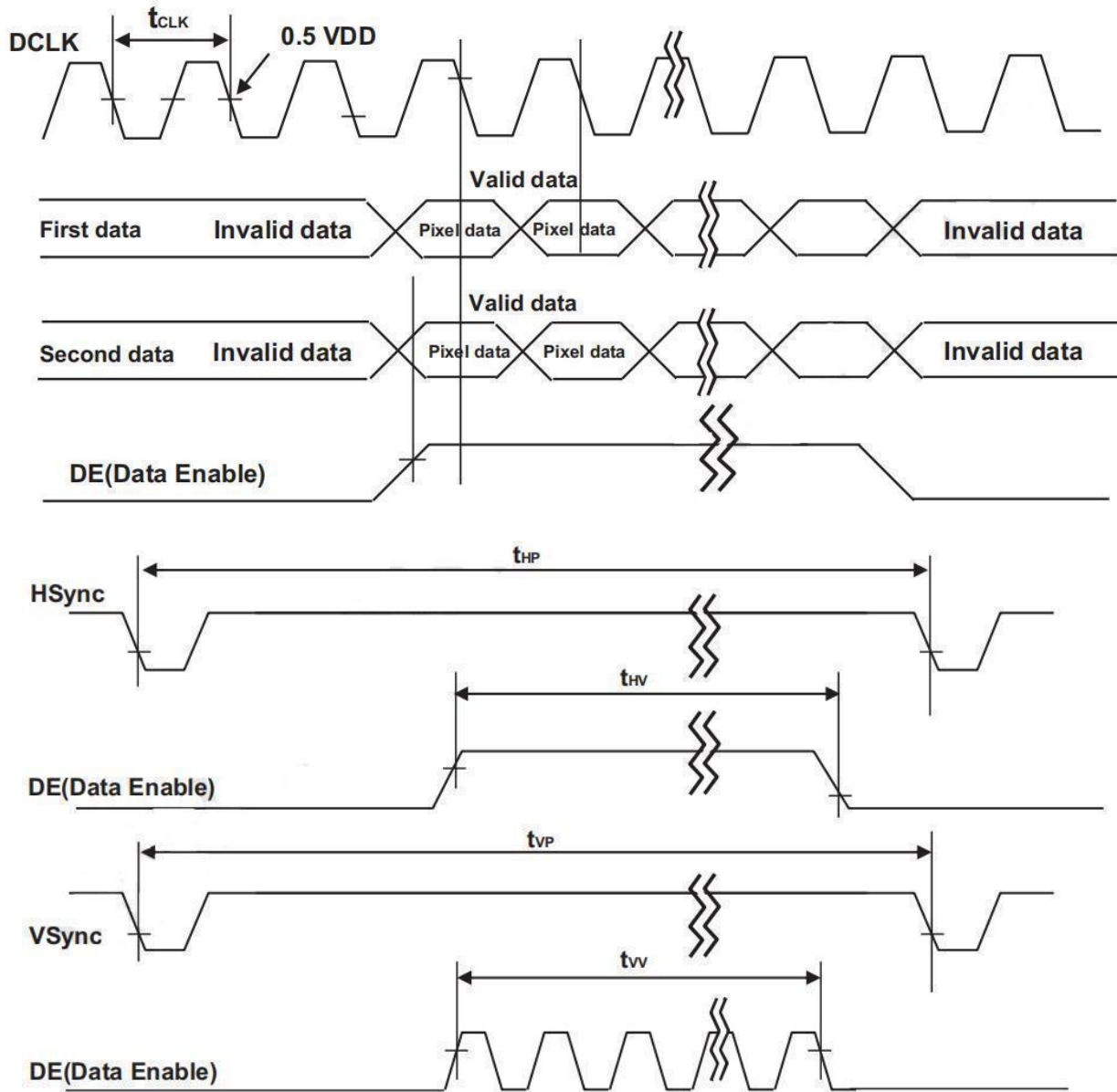
Item		Symbols	Min	Typ	Max	Unit	
Clock	Frequency	1/Tc	58	74.25(92.8)	97	MHz	
	High Time	Tch	-	4/7Tc	-		
	Low Time	Tcl	-	4/7Tc	-		
Frame Period		TV	1100	1125	1149	lines	
			47	60(75)	78	Hz	
Horizontal Active Display Term		Valid	tHV	-	960	-	tCLK
		Total	tHP	1060	1100	1200	tCLK
Vertical Active Display Term		Valid	tVV	-	1080	-	tHP
		Total	tVP	1100	1125	1149	tHP

Notes : This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

<Table 6. LVDS Inout SSCG>

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F	LVDS Input frequency	-	58	74.25(92.8)		MHz
TLVSK	LVDS channel to channel skew	F=100MHz VIC=1.2V VID=±200mV	-(1/F)*30%	-	+(1/F)*30%	ps
FLVMOD	Modulating frequency of input clock during SSC	F=85MHz VIC=1.2V VID=±200mV	0	-	200	KHz
FLVDEV	Maximum deviation of input clock frequency during SSC		-3	-	+3	%
TCY-CY	Cycle to Cycle jitter		-	-	50	ps

5.2 Signal Timing Waveform



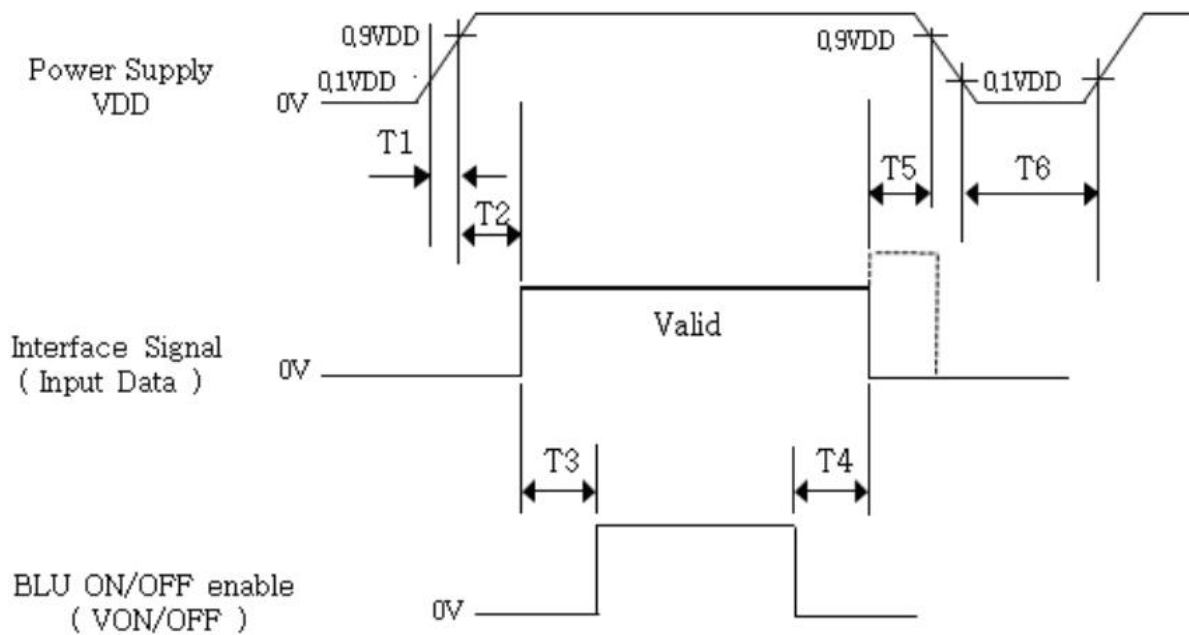
5.3 Input Signals, Basic Display Colors and Gray Scale of Colors

<Table 7. Input Signal and Display Color Table>

Color & Gray Scale		Input Data Signal																							
		RED Data								GREEN Data								BLUE Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Magen	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
	Yello	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	△	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	▽	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	RED	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0		
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0		
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0		
	▽	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0		
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0		
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
Gray Scale of White	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	△	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1		
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1		
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Bright	1	1	1	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	
	▽	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

5.4 Power Sequence

To prevent a latch-up or DC operation of the Open Cell, the power on/off sequence shall be as shown in below



<Table 8. Sequence Table>

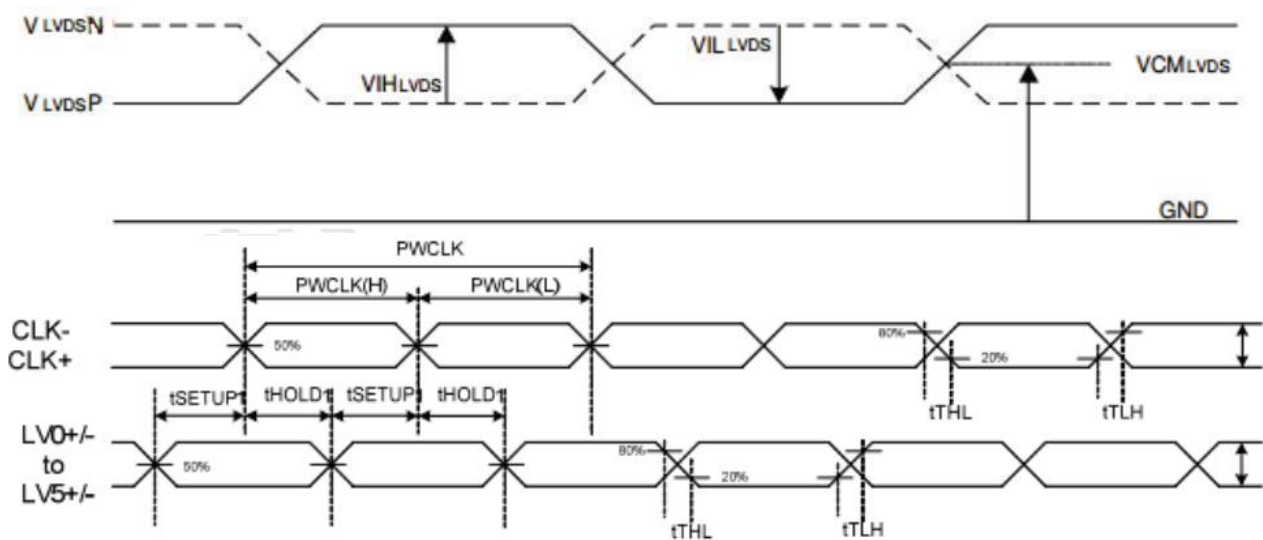
Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	20	ms
T2	0	-	-	ms
T3	200	-	-	ms
T4	100	-	-	ms
T5	0	-	-	ms
T6	1	-	-	ms

Notes: 1. Back Light must turn on after power for logic and interface signal are valid.
Even though T1 is out of SPEC, it is still ok if the inrush current of VDD is below the limit.

6. Mini-LVDS Signal Specifications

<Table 9. Timing Table>

Symbol	Parameter	Min	Typ	Max	Units
FM	Mini-LVDS Clock frequency	-	-	400	MHz
FMLVMOD	Modulating frequency of input clock during SSC	-	-	600	KHz
FMLVEDV	Maximum deviation of input clock frequency during SSC	-3	-	+3	%
VIHLVDS	Mini-LVDS high input voltage	200	-	-	mV
VILLVDS	Mini-LVDS high input voltage	-	-	-200	mV
tSETUO	Data setup time	0.5	-	-	ns
tHOLP	Data hold time	0.5	-	-	ns



7. Optical Specifications

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature $= 25 \pm 2^\circ\text{C}$) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0° . We refer to $\theta=0$ ($=\theta_3$) as the 3 o'clock direction (the "right"), $\theta=90$ ($=\theta_{12}$) as the 12 o'clock direction ("upward"), $\theta=180$ ($=\theta_9$) as the 9 o'clock direction ("left") and $\theta=270$ ($=\theta_6$) as the 6 o'clock direction ("bottom"). While scanning θ and/or Φ , the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 1.2.0V $\pm 10\%$ at 25°C . Optimum viewing angle direction is 6 o'clock.

<Table 10. Optical Table>

[VDD = 12.0V, Frame rate = 60Hz, Ta = $25 \pm 2^\circ\text{C}$]

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	θ_3	CR > 10	89	-	Deg.	Note 1
		θ_9					
	Vertical	θ_{12}					
		θ_6					
Contrast ratio	CR		900:1	1200:1	-		Note 2
Reproduction of color	White	Wx	$\theta = 0^\circ$ (Center) Normal Viewing Angle	TYP. - 0.03	TYP. + 0.03		Note 3 (With BOE BLU)
		Wy					
	Red	Rx					
		Ry					
	Green	Gx					
		Gy					
	Blue	Bx					
		By					
Response Time	G to G	Tg	-	8	10	ms	Note 4
Gamma Scale			2.0	2.2	2.4		
Cell Transmittance				5.0		%	Note 5

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of = 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See Figure 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in Table 9 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel. The BLU is used by BOE.
4. Response time Tg is the average time required for display transition by switching the input signal as below table and is based on Frame rate fV =60Hz to optimize. Each time in below table is defined as Figure 2 and shall be measured by switching the

Measured Response Time	Target																
	0	15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255
0																	
15																	
31																	
47																	
63																	
79																	
95																	
111																	
127																	
143																	
159																	
175																	
191																	
207																	
223																	
239																	
255																	

5. Definition of Transmittance (T%) :

Module is with white(L255) signal input

$$\text{Transmittance} = \frac{\text{Luminance of LCD Module}}{\text{Luminance of BLU}} \times 100 \%$$

8. Mechanical characteristics

8.1 Dimensional Requirements

Figure 3 (located in Appendix) shows mechanical outlines for the model HV320FHB-N02. Other parameters are shown in Table 10.

< Table 11. Dimensional Parameters >

Parameter	Specification	Unit
Active area	689.4(H) x 392.85(V)	mm
Pixel pitch	121.25(H) x RGB x 363.75(V)	μm
Number of pixels	1920(H) x 1080(V) (1 pixel = R + G + B dots)	piels
Weight	-	gram

8.2 Semi-Glare and Polarizer Hardness

The surface of the LCD has an Anti-glare coating to minimize reflection and a coating to Reduce scratching.

9. Reliability Test Condition

< Table 12. Reliability Test Condition >

Item	Test Condition
High-Temp/STG	Ta = 60 °C, 240 hrs
Low-Temp/STG	Ta = -20 °C, 240 hrs
High-Temp/HMD	Ta = 50 °C, 80%RH, 240hrs
High-Temp/OP	Ta = 50 °C, 240hrs
Low-Temp/OP	Ta = 0 °C, 240hrs
TST	Ta = -20 °C ↔ 60 °C (0.5 hr), 100 cycle

10. Backlight Unit

10.1 LED Pin Assignment

it includes 144pcs (4014) LED in theLED light bar.(8 strings and 18 pcs LED of one string)

connector CN2 : PH- 2P *1

Pin	Signal Name
1	VDD- (Black)
2	VDD+ (Red)



10.2 Recommended Operating Condition

(Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit
LED operation Voltage	V_{led}	50.4	-	61.2	V
LED operation Current	I_{led}	-	480	-	mA
Backlight Power	P_{BL}	24.19	-	29.37	W
Luminance	L	240	300		nit
LED Life Time		30000			Hrs
Luminance uniformity	ΔL	75	80		%

11. Appendix

Figure 1. Measurement Set Up

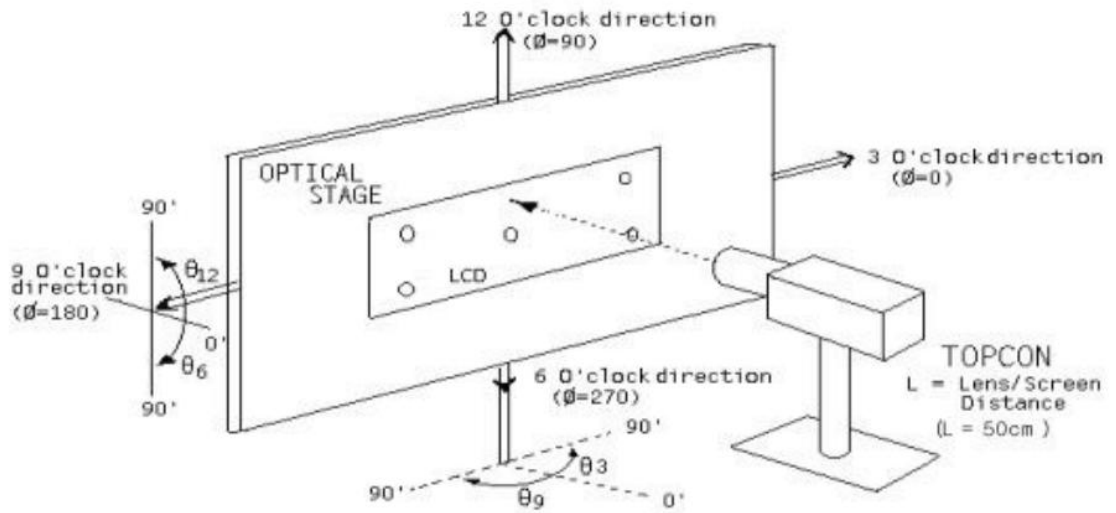


Figure 2. White Luminance and Uniformity Measurement Locations(9 points)

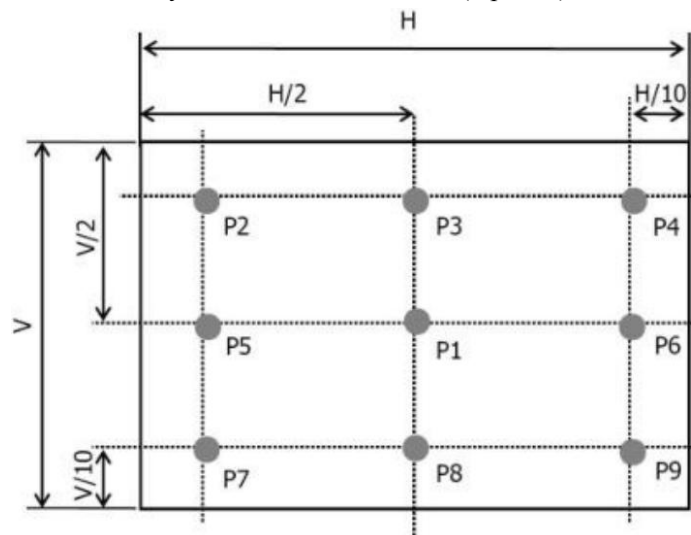


Figure 3. Response Time Testing

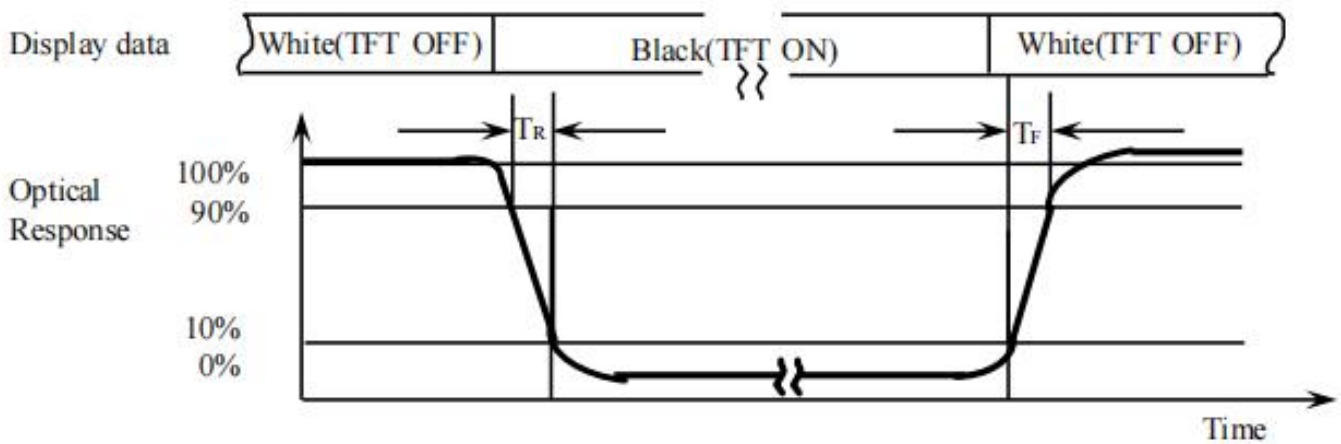
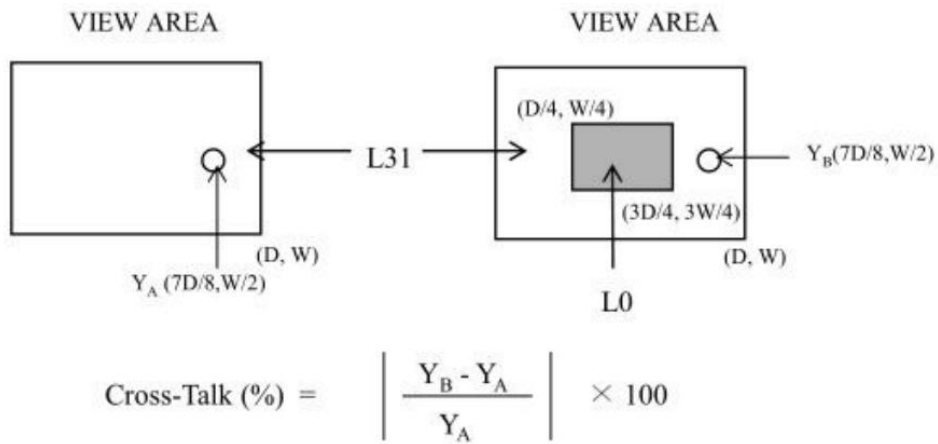


Figure 4. Cross Modulation Test Description



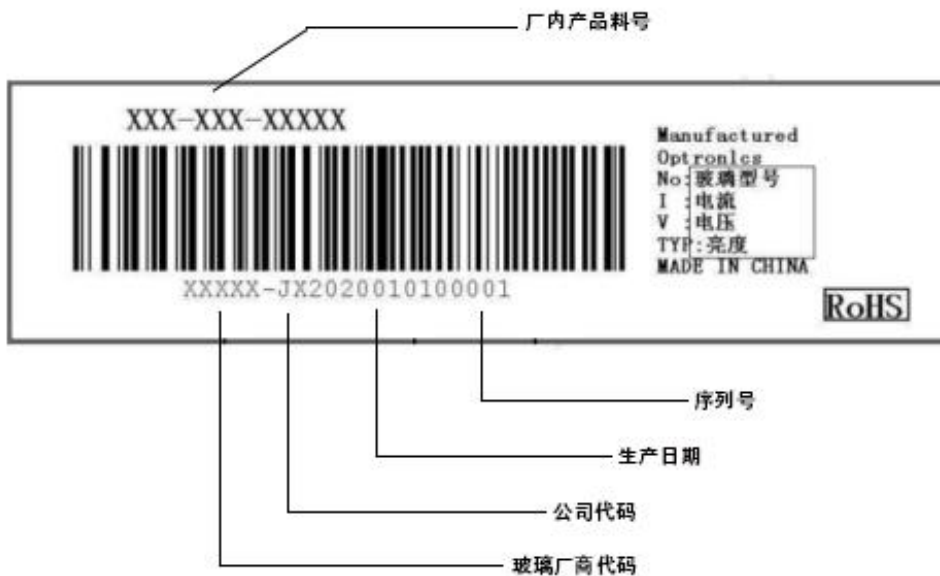
Where : Y A = Initial luminance of measured area (cd/m²)

Y B = Subsequent luminance of measured ared (cd/m²)

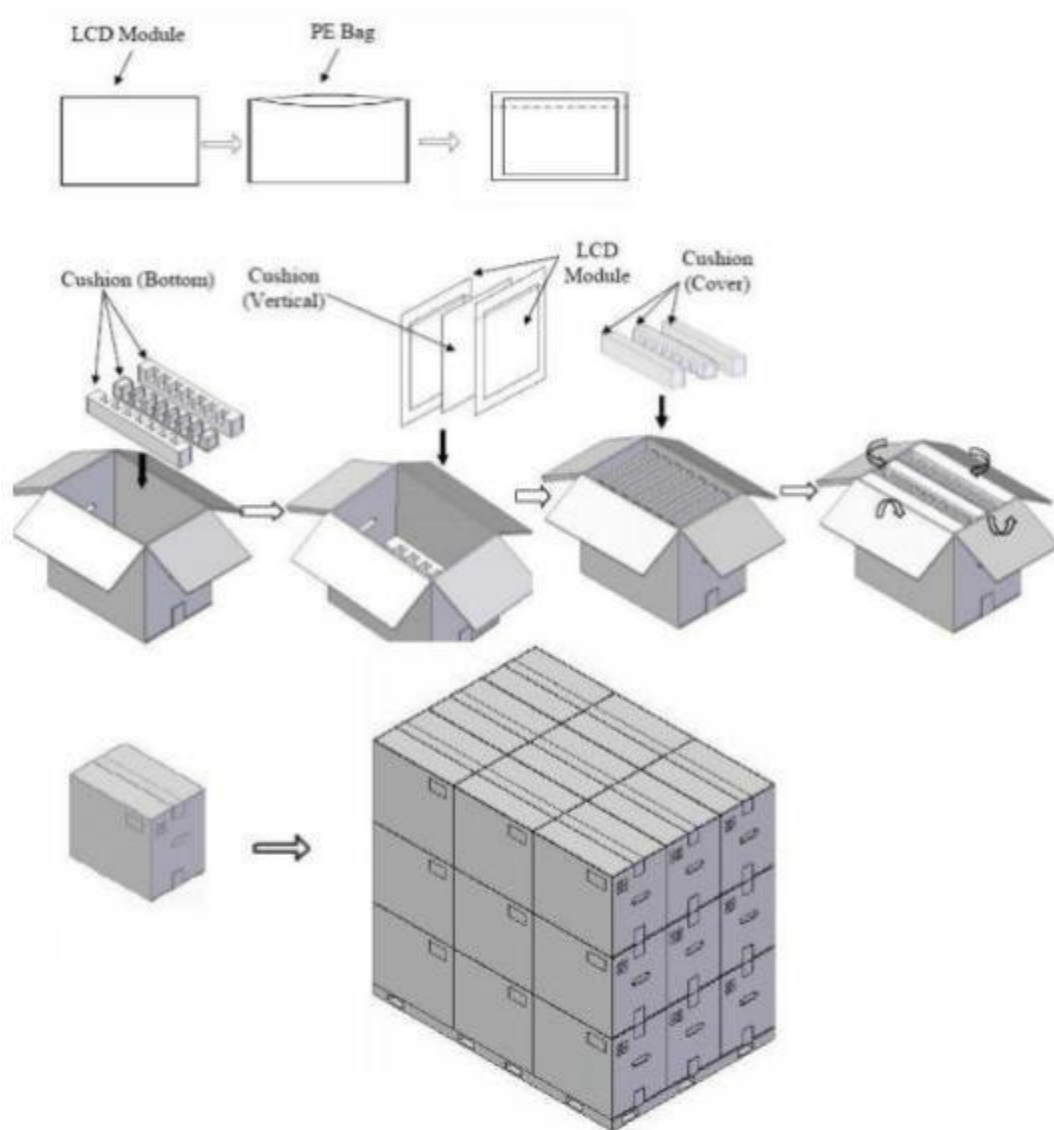
The location measured will be exactly the same in both patterns

12. Shipping Label

The label is on the panel as shown below



Parameter	Packing box	Unit
Size	810(L)x230(W)x480(H)(typ.)	mm
Weight	1.367(typ.)	Kg
Total weight	13.76(typ.) (with 10 products)	Kg



13. Precaution

13.1 Assembly and handling precautions

1. Do not apply rough force such as bending or twisting to the module during assembly.
2. To assemble or install module into user's system can be in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
3. It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.
4. Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
5. Do not pull the I/F connector in or out while the module is operating .
6. Do not disassemble the module. Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very
6. soft and easily scratched.
7. It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.
8. High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
9. When ambient temperature is lower than 10 °C may reduce the display quality. For example, the response time will become slowly.

13.2 Safety precautions

1. It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
2. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth, in case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
3. After the module's end of life, it is not harmful in case of normal operation and storage.

